

## Your Alumni Newsletter

This newsletter is a continuation of the previous one where we featured our alumni working at Intel. We have a few additions in this issue. We also have information on other ASU electrical engineering alumni.

Note the new newsletter name: ECEE Connections. The School Director will explain about the change in his message below.

Do you have an idea for a future issue of ECEE Connections? Let me know at [joseph.palais@asu.edu](mailto:joseph.palais@asu.edu).

Thanks,  
Joseph Palais  
ECEE Graduate Program Chair



Above: Intel's latest factory - Fab32, Chandler, AZ



## Rushit Shah

*Product Development Engineer*

Rushit Shah graduated with an MSE in May 2003. He works at Intel as a product development engineer, developing test programs for enabling high volume manufacturing of latest generation microprocessors. Shah's work involves identifying timings and levels for different test content supported by the test program, and developing and implementing thermal testing of processors. He is responsible for validating thermal related issues and inspecting thermal specs for the processors as well as quality, yield, and reliability. He believes that ECEE has a distinguished group of professors: Dr. Dieter Schroder, Dr. Chaitali Chakrabarti, Dr. David Allee and Dr. Andreas Spanias, all instructors for his ASU courses. He believes his ASU courses were very well focused on educating students and solidifying the fundamentals of engineering. He is appreciative of his ASU education for having taught him his engineering skills and for helping him grow as a person.

## Nicholas Peña

*Device Engineer*

Nicholas Peña graduated from ECEE with an MSE in solid state devices in fall 2000. While at ASU, he particularly cites Dr. Schroder's classes as very beneficial to his current job at Intel. Dr. Schroder's teaching methods helped Peña understand the concepts needed in his current role. After being interviewed at an ASU job fair, Peña was hired in January 2001 to work for Intel at the Rio Rancho Facility (Fab11) as part of its Rotation Engineers Program (REP), where he took on the position of Device Engineer. Peña feels that being an ASU graduate was very beneficial to his career because of the respect that ASU garners in the semiconductor industry.



## Message from the School Director



EE Alums,

The reconstructing of the Fulton Schools of Engineering that I mentioned in the last newsletter has been fully implemented. Your Electrical Engineering programs remain the core mission of our new School of Electrical, Computer and Energy Engineering. The focus of this issue of ECEE Connections on Alumni at Intel is an example of the computer component of the new name of the school. We look forward to hearing from you about all of your successes.

Stephen M. Phillips  
Professor and Director



### Kenneth Williamson

Kenneth Williamson graduated in spring 2007 with an MSE. During his 10 years at Intel, Williamson held a number of positions, including product engineer, test engineer, RTL design validation engineer, and physical design engineer. As a product and a test engineer, his duties involved creating software capabilities to monitor the post-silicon quality of Pentium micro-processors produced in Intel Fabs located worldwide. The ultimate goal was to develop and refine test programs so that as a new product matured in the Fabs, each die would be validated as rapidly as possible while guaranteeing that each unit met Intel's published performance specs.

As an RTL design validation engineer, Williamson used his knowledge of hardware design languages (HDL) and synthesis concepts learned at ASU to write tests, debug logic problems, and verify HDL code to meet functional and timing requirements. As a physical design engineer, he was concerned with defining physical layout and simulating circuit performance on silicon such that the chip performed within specifications once it was fabricated. His advisor was Dr. Dieter Schroder, whose depth of knowledge and friendly personality, are fondly remembered and appreciated by Williamson. He believes an MSE from ASU and a solid state devices and design process background were instrumental for an opportunity to interview with Intel. Currently, Williamson is employed at Marvell Semiconductors in Arizona.

### Dongqiang Wu

#### *Sr. Product Development Engineer*

Dongqiang Wu graduated with an MSE in 2000. He is currently employed at Intel as a senior product development engineer working for the embedded products group. His team creates and modifies Intel architecture of silicon chips to fit the embedded industry's special needs as there is currently a high demand for semi-conductors. Wu has received many divisional recognition awards for his valuable contributions in product development. While working for Motorola, his technical capabilities boosted the company's R&D efforts. He is grateful for the knowledge he acquired from his MSE advisor, Dr. Dieter Schroder. Wu feels that graduating from ASU provided him with a unique opportunity to increase his knowledge of solid state devices; it also helped him grow professionally with Intel Corporation.

### Ezra Williams



Ezra Williams graduated in 1997 from ECEE with a BSE degree. He is currently employed by Intel in Chandler, AZ, as a product marketing manager. Williams has been with Intel since 2001 in various positions: silicon validation engineer, platform applications engineer and currently, a position in product marketing. Williams leads the product marketing effort for processors used in the embedded and communications market segments. In this diverse role, requiring technical and business knowledge, his responsibilities include driving completion of product lifecycle milestones, customer requirements, product forecasting, pricing analysis, collateral development, launch planning, sales training and customer engagements.

Williams has completed an MBA program, received numerous divisional awards for contributions to launched products and completed various technical and non-technical courses that have all been helpful in fostering career growth. He believes his advisor, Dr. Joseph Palais, was extremely helpful in assisting him in his senior project in fiber optic communications systems. "Graduating from ASU with an EE degree gave me a solid engineering foundation, which I have used in my 12- year career at two Fortune 500 technology companies (Hewlett Packard & Intel) in various engineering and business/marketing roles," says Williams.

### Mark Stapp

Stapp received a BSE from ASU in May 1991. While at ASU, Stapp enrolled in numerous courses taught by Dr. Richard Farmer; he considers Dr. Farmer's dedication and teaching style one of the driving factors that led him to pursue Power Engineering. As a junior, Stapp was unsure of whether to pursue a career in solid state, communications or power, so he decided to take Dr. Farmer's power system analysis class. Dr. Farmer's love of teaching and care for his students sparked Stapp's interest in power that semester. Stapp extends his gratitude to ASU and Professor Farmer for truly caring about student education. Stapp is currently an engineering and operations director at Greenville Electric Utility System in Greenville, Texas.

## Lesley Polka and Dustin Wood



Lesley Polka and Dustin Wood are both ECEE graduates employed by Intel. Polka graduated with a BSE in 1987, MS in 1989 and a PhD in 1995; Wood graduated with a BS in 1996 and an MS in 1997. Polka has been with Intel for 15 years, and currently is an electrical packaging engineer. She works in Intel's Assembly and Test Technology Division (ATTD) on technology development for microprocessor packaging, dealing with electrical challenges and packaging requirements for Intel's future microprocessors. Her focus is on technologies and products that are 4-6 years out in Intel's production roadmap. Some of the more

interesting areas that she has worked on in the last few years has included wireless packaging, high-density/high-speed packaging for very high bandwidth applications, and microprocessor sockets to meet Intel's electrical requirements for its next-generation products. Interestingly, Polka was part of a small team from Intel's packaging organization that worked collaboratively with ASU to develop and co-teach a packaging class offered through the School's materials science program. Polka has been a guest speaker for undergraduate engineering classes, and says she is always eager to return to ASU to share her work experiences with the next-generation of engineers.

Wood has been with Intel for 12 years and is currently an analog design engineer in the System-on-a-Chip Enabling Group (SEG). He is responsible for delivering electrically robust, production-quality circuit systems for Intel's mainstream chipset products. The most recent of these was the Intel Core i3 processor, scheduled for launch in Janu-

ary 2010. Wood has also received the Intel Achievement Award, the highest individual honor at Intel, for working on a project on innovative power delivery solutions for the Pentium4 processor. Wood has had 19 of his ideas patented and has nine patents currently pending. He is also a Senior Member of IEEE.

Polka believes all of her ASU professors were great mentors, teachers, and researchers. Wood's most memorable class, Characterization of Semiconductor Devices, was taught by Dr. Dieter Schroder. The class provided Wood with his first real glimpse into his future career in electrical engineering. They both believe that ASU has offered them a solid platform in electrical engineering upon which to build their careers. Polka and Wood met at Intel. They have been married for 6 ½ years; have a combined 27 years experience at Intel; and have 5 ASU ECEE degrees. They also have a 5 ½ year-old daughter, who says she wants to attend ASU and work at Intel.

## Jo Davidson

Jo Davidson is a 1963 graduate of the USAF Airmen Education Commissioning Program at ASU. He also received an MS in Engineering from Suffield University in 2006. During his time at ASU, Davidson's advisor, Mr. Steinman, required him to take a course in feedback control systems, where Davidson gained enough knowledge to write a 200-line Fortran program while working for Eastman Kodak Company in Rochester, NY. He believes that he was the first person in the country to utilize the Leverrier-Fadeev algorithm for solving inverse Laplace transform equations to plot time response, frequency response, and root locus diagrams of any feedback control system consisting of elements described as functions of using piecewise linear inputs

Davidson went on to become a senior systems engineer, designing microwave, cellular, satellite, and packet switched networks as well as wired and wireless LANs. Davidson also designed a satellite communications network for the Philippine Long Distance Telephone Company; he was Project Manager for BOFANET; and he installed and tested a network linking 400 ATM machines to Citibank hosts in New York City using x.25 protocol while working for NCR Comten in St. Paul, Minnesota.

## Rachana Maitra

Rachana Maitra received an MS degree from ASU in 1999. She worked at Intel from June 1999 until November 2007. Maitra is currently employed at Marvell Semiconductors in Arizona.

## Arun Subbiah

Arun Subbiah graduated in 1995 from ASU. Subbiah is currently a Principle Engineer at Intel.

## ASU ECEE Intel Employees

*(not previously acknowledged)*

Mary Jo Rack  
Steve Ramey  
Lucian Shifren  
Steven Sowinski

*Keep in touch with ECEE. Please e-mail your career updates to [askee@asu.edu](mailto:askee@asu.edu)*

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## Celebrate Your Alumni Status

### Electrical Engineering Alumni Newsletter

This publication is written, designed and produced by the School of Electrical, Computer and Energy Engineering of the Ira A. Fulton Schools of Engineering at Arizona State University for distribution to alumni, industry partners and academic friends worldwide.

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We invite you to celebrate and honor your alumni status by keeping in-touch with the School of Electrical, Computer and Energy Engineering at ASU.


Check out our webpage for news and information about our faculty, our students, and our programs. We are located at: <http://engineering.asu.edu/ecee>

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- Mail your gift to – ASU Foundation, Gift Processing, PO Box 2260, Tempe, AZ 85280-2260. Check should be payable to "ASU Foundation" with "Electrical Engineering" noted on the memo line.

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