Course (Catalog) Description:
Develop digital logic with modern practices of hardware description languages. Emphasizes usage, synthesis of digital systems for programmable logic, VLSI.
Lecture, laboratory.
Required for majors in bioengineering, computer systems engineering, and electrical engineering.

Prerequisites:
EEE 101 (or equivalent), CSE 120 or EEE 120.

Textbook:
D. J. Smith, *HDL Chip Design: A practical guide for designing, synthesizing, and simulating ASIC’s and FPGA’s using VHDL or Verilog*, Doone Publications.

Supplemental Materials:
Xilinx CPLD and FPGA design notes.

Prerequisites by topic:
1. Digital design fundamentals: Logic gates and boolean logic.
2. Sequential circuit fundamentals: State machines and sequential logic.
3. Basic programming skills: Procedural programming in C.

Topics:
1. Verilog language fundamentals and operation.
2. Mapping HDL constructs to hardware components and synthesizable verilog.
3. Programmable logic architectures and circuits.

Course Objectives:
1. Students can design digital circuits using a hardware description language and synthesis.
2. Students understand modern programmable logic devices and can use them in practical applications.
3. Students understand timing and effects of hardware mapping and circuit parasitics.

Course Outcomes:
1. Students can apply logic fundamentals using hardware description languages.
2. Students understand the difference between procedural programming and hardware description languages.
3. Students can write synthesizable verilog code describing basic logic elements
   a. Combinatorial logic.
   b. Sequential logic.
4. Students can code state machines in a hardware description language.
5. Students can analyze and develop basic logic pipelined machines.
6. Students understand basic programmable logic architectures.
7. Students can synthesize working circuits using programmable logic.
8. Students understand sequential and combinatorial logic timing.
9. Students understand the impact of actual routing and circuit parasitics.

Course Topics:
1. Review logic fundamentals, gates, latches, flip-flops and state machines (2 weeks).
2. Verilog HDL fundamentals, simulation, and test-bench design (4 weeks).
3. Synthesizable code and hardware/HDL mapping (3 weeks).
   a. Basic logic.
   b. Sequential circuits.
   c. Arithmetic circuits.
4. CPLD architecture and synthesis (3 weeks).
5. FPGA architecture and synthesis (4 weeks).

Computer Usage:
Modelsim and FPGA synthesis tools.

Laboratory Experiments:
Students meet weekly for a three-hour laboratory under the guidance of a TA.

Assessment:
Through homeworks, quizzes, tests, project and final exam.
Distribution of Weights:
Homeworks: up to 15%, Quizzes: up to 15%, Tests: up to 20%, Laboratory: up to 25%, Final exam: up to 25%

Course Contribution to Engineering Science and Design:
EEE 333 contributes to engineering science through logic design, problem solving, and computer solutions.

Course Relationship to Program Objectives and ABET Outcomes:
b: Significant laboratory experience
c: Significant design experience.
d: Laboratory teams feature various engineering majors.
e: Students are taught problem solving methodologies with applications to real-world, engineering problems. Some modeling within test-bench design.
k: Logic design, HDL coding, and synthesis skills are needed in industry. Use of modern Modelsim and FPGA synthesis software.

Person preparing this description and date of preparation: Lawrence T. Clark, K. Tsakalis, Apr. 2009.