GaN-on-Si Switch Mode RF Power Amplifier for non-constant envelope signals:

In today’s LTE centric communication era, signals with large Peak-to-Average Power Ratio (PAPR) has made the transmitter design, specifically the Power Amplifier Design a big challenge. Apart from high PAPR, the need for high efficiency and high linearity is more than ever. With devices getting smaller the need for long battery life has mandated high efficiency. With the requirement of simultaneous audio, video and high speed broadband data, the need for large signal bandwidth has caused the spectrum congestion. This has increased the chances of information distortion and hence linearity is of utmost importance. With these stringent requirements the Digital transmitter architecture has gained quite a lot of momentum in recent times. The main motivation behind the use of digital transmitter apart from the ease of DSP implementation is the use of the highly efficient Switch Mode Power Amplifier which potentially can reduce the overall size and increase the battery life. However the generation of excessive harmonics along with the required frequency has generated linearity issues rendering switch mode PAs difficult to implement. Also, the incapability of switch mode power amplifiers to efficiently amplify modern day non-constant envelope signals like WCDMA, LTE has posed another challenge and has necessitated the deployment of complicated digital modulation schemes like sigma-delta and RF pulse width modulation. With the innovation in solid state device physics, high performance compound III-V semiconductors like GaN/GaAs are achieving performances which were considered impossible in the past. With the success at device level Switch Mode Power Amplifiers have immense potential of overcoming the conventional LDMOS Doherty-DPD based linear Power Amplifiers for BTS.

This thesis proposes several GaN-on-Si based switched mode amplifiers for implementation in the modern day Digital transmitter architecture. It compares 3 different architectures and justifies their deployment under certain practical issues like effect of devices package inductance, bond-wire effect. The three architectures are Current-Mode Class-D, Push-Pull Class-E and Inverse Push-Pull Class-E. Apart from being efficient some of the architectures are more tolerant to component variations, frequency and duty cycle variations. These PAs are targeted for femto-cell applications at 900MHz and outputs power in the range of 4-6W. All these architectures are over 60% efficient at nominal 50% duty cycle input but the third architecture is more tolerant to high PAPR signals (manifested as reduced duty-cycle at the input). This work compares the 3 architecture in simulation as well on the board level. The PAs are designed using GaN-on-Si Nitronex devices, a MMIC with differential devices with pre-drivers in it. The PCB is designed on a FR-4 material with 50-ohm matching using a coplanar waveguide approximation. The PAs are differentially driven using a broadband amplifier and a broadband Balun (both off chip) by square wave as well as over-driven sine wave.