Abstract
Memories play an integral role in today’s advanced ICs. There is a need for increased storage within smaller area. Technology scaling has enabled this but at the price paid for variability and reliability impacts arising due to the smaller and smaller geometry devices. This in turn calls for accurate method or techniques to measure and extract the variability in the SRAM cell to account for and predict the performance metrics of the future memory design in the nano scale regime. In this work, a novel test measurement and extraction technique is presented which is non-invasive to the actual operation of the SRAM memory array. The salient features of this work include i) A single ended SRAM test structure with no disturbance to SRAM operations ii) a convenient test procedure that only requires quasi-static control of external voltages iii) non-iterative method that extracts the $V_{TH}$ variation of each transistor from eight independent switch point measurements.

With the present day technology scaling, in addition to the variability with the
process, there is also the impact of other aging mechanisms which become dominant. The various aging mechanisms like Negative Bias Temperature Instability (NBTI), Channel Hot Carrier (CHC) and Time Dependent Dielectric Breakdown (TDDB) are critical in the present day nano-scale technology nodes. In this work, we focus on the impact of NBTI due to aging in the SRAM cell and have used the log(t) based Trapping/De-trapping model to explain the shift in threshold voltage $V_{TH}$. The aging section focuses on the following i) Impact of Statistical aging in PMOS device due to NBTI dominates the temporal shift of SRAM cell ii) Besides static variations, shifting in $V_{TH}$ demands increased guard-banding margins in design stage iii) Aging statistics remain constant during the shift, presenting a secondary effect in aging prediction. iv) We have also tried to see if the aging mechanism can be leveraged to be used as a compensation technique to reduce mismatch due to process variations.

Finally, the entire test setup has been tested in SPICE and also validated with silicon and the results are presented. The method also facilitates the study of design metrics such as static, read and write noise margins and also the data retention voltage and thus help designers to improve the cell stability of SRAM.