Abstract

Semiconductor device scaling has kept up with Moore's law for the past decades and they have been scaling by a factor of half every one and half years. Every new generation of device technology opens up new opportunities and challenges and especially so for analog design. High speed and low gain is characteristic of these processes and hence a trade off that can enable to get back gain by trading speed is crucial. This thesis proposes a solution that increases the speed of sampling of a circuit by a factor of three while reducing the specifications on analog blocks and keeping the power nearly constant. The techniques are based on a recently published switched capacitor technique called Correlated Level Shifting. A triple channel Cyclic ADC has been implemented, with each channel working at a sampling frequency of 3.33MS/s and a resolution of 14 bits. The specifications are compared with that based on a traditional architecture to show the superiority of the proposed technique.