Digital architectures for data encryption, processing, clock synthesis, data transfer, etc. are susceptible to radiation induced soft errors due to charge collection in complementary metal oxide semiconductor (CMOS) integrated circuits (IC’s). Radiation hardening by design (RHBD) techniques such as double mode redundancy (DMR) and triple mode redundancy (TMR) are used for error detection and correction respectively in such architectures. It is a challenge to maintain the efficacy of these techniques while employing them in mission critical applications as the overhead (hardware and timing) is simultaneously sought to be minimized. Multiple node charge collection (MNCC) causes domain crossing errors (DCE) which can render the redundancy ineffectual. This dissertation studies the effect of DMR and TMR hardening and proposes techniques to ensure DCE mitigation with statistical confidence for various architectures. Both
sequential and combinatorial logic are separated using these custom and computer aided design (CAD) methodologies.

Radiation vulnerability and design overhead are studied on VLSI sub-systems including an advanced encryption standard which is DCE mitigated using module level coarse separation on a 90-nm process. Specialized placement regions (fences) are explored to achieve the desired spatial separation. A radiation hardened microprocessor (HERMES2) is implemented in both 90-nm and 55-nm technologies with an interleaved separation methodology. A DMR register-file (RF) is implemented in 55 nm process and used in the HERMES2 microprocessor. The RF array custom design and the decoders APR designed are explored with a focus on design cycle time. Quality of results (QOR) is studied from power, performance, area and reliability (PPAR) perspective to ascertain the improvement over other design techniques.

A radiation hardened all-digital multiplying pulsed delay locked loop (DLL) is designed for double data rate (DDR2/3) applications for data eye centering during high speed off-chip data transfer. The effect of noise, radiation particle strikes and statistical variation on the designed DLL are studied in detail. Vulnerability of the non-hardened design is characterized and portions of the redundant DLL are separated in custom and auto-place and route (APR). Portions of the critical timing circuits of the DLL i.e. the coarse and the fine delay units are fabricated on a 55-nm low power process. Thus, a range of designs for mission critical applications are implemented using novel methodologies proposed in this work and their potential PPAR benefits explored in detail.