

****Disclaimer****

This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class. Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.



EEE 498/591

Constructionist Approach to Microprocessor Design

TBD



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ISTB4 551C

Office Hours: TBD

The syllabus will be updated, as needed, through course announcements on blackboard and piazza. All students are responsible for the contents of those announcements.

Course Description: Constructionist learning is about organic discovery and exploration. In this course we will explore the principles of microprocessor design by iteratively implementing a more and more complicated design.

Prerequisite(s): EEE 333 Hardware Design Languages
Students should be comfortable with Verilog, Simulation, Verification, and Synthesis.

Units: 4

Text: *Computer Organization and Design* (5th Ed.),

Author: David A. Patterson, John L. Hennessy ;

ISBN-13: 978-0124077263

Learning Objective: Students should be able to

1. Work on large HDL design
2. Work iteratively on a large HDL design
3. Verify a large HDL design
4. Effectively communicate issues in hardware design
5. Discuss design trade-offs in terms of physical cost and design effort
6. Discuss the operation of a microprocessor from the SW perspective
7. Discuss the operation of a microprocessor from the HW perspective

Course Topics:

1. Microprocessor physical design
2. ISA
3. Pipelined execution
4. Memory Hierarchy
5. Branch Prediction
6. Exceptions
7. Virtual Memory
8. Instruction Level Parallelism
9. Data Level Parallelism

Grade Distribution (No Curve):

Projects	50%
Quizzes	30%
Final Exam	20%

Grade Scale:

A+	> 97%
A	> 93%
A-	> 90%
B+	> 87%
B	> 83%
B-	> 80%
C+	> 77%
C	> 70%
E	≤ 70%

Reading: Reading will be assigned during lecture. The reading assigned during a lecture is indicated on the lecture plan. This reading should be done before the next lecture. You are responsible for the material in the reading not covered in lecture.

Project: There will be several assignments which will cover the design of a microprocessor using modern EDA tools. Each project will ask you to implement some feature of a microprocessor discussed in class, verify its functionality, vary a design parameter, report on the synthesized design, and write a short report. All project work will be done in pairs. You should adopt pair programming techniques. Each individual is responsible for the joint work. Note that the work you submit should belong to you and your partner, we will use procedural tools to detect plagiarism in your code. The final project in the course will task you with improving the performance of your microprocessor by adding an advanced feature (eg. register renaming or dynamic scheduling).

Quizzes: Every week we will have a 20 minute quiz at the beginning of class on Wednesday covering the prior week's material. This will usually be 1-3 quick questions to provide feedback on your progress in the class. These quizzes will also help me to identify misconceptions that we can address the following week. There will be no make-up quizzes or alternate exam times, but the lowest quiz grade will be dropped.

Exam Schedule: The final will be held during the time designated by the registrar. Exams are closed notes, closed books, closed electronic device. You may bring a double sided sheet of paper with hand written notes for the final. Those "cheat sheets" should be your own work. Alternate

exam times must be scheduled in advance, there will be no make-up exams.

Regrade Requests: You may request a regrade from me up to one week (168 hours) after receiving your graded assignment. You should submit your regrade in my office hours or to my mail box. Your regrade request should be written as a cover letter on top of your assignment. The probability of receiving points in a regrade request is inversely proportional to the length of the regrade request note.

Piazza: We will use piazza in place of blackboard's bulletin board. You should use this to ask me and your peers questions about course topics, the homework, lab, lab materials, etc. The students who consistently provide good answers to their peers will receive bonus points toward their final grade.

Communication Policy: All questions that are not personal in nature should be posted on Piazza. Please feel free to email otherwise. All communication (Piazza, email to the course staff, email to eachother) should be professional in nature.

Honor Code: Each student has an obligation to act with honesty and integrity, and to respect the rights of others in carrying out all academic assignments. There is a University honors policy (<https://provost.asu.edu/sites/default/files/AcademicIntegrityPolicyPDF.pdf>). There is also a Fulton Schools of Engineering honor code (<http://engineering.asu.edu/integrity/honor-code/>). If you have not already read and understood them, you should do so.

Students with Disabilities: The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. One element of this legislation requires that all qualified students with documented disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation please contact the Disability Resource Center (<https://eoss.asu.edu/drc>) DRC@asu.edu 480-965-1234

Data for Research Disclosure: Any and all results of in-class and out-of-class assignments and examinations are data sources for research and may be used in published research. All such use will always be anonymous.

Online Resources: There are a number of useful online resources.

- *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling* (2nd Edition), **Author:** Stuart Sutherland, Simon Davidmann, Peter Flake ; **ISBN-13:** 978-0-387-36495-7 ASU Lib
- *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* (1st Edition)¹, **Author:** Chris Spear ; **ISBN-13:** 978-0-387-27038-8 ASU Lib
- *Learning Perl* (6th Edition), **Author:** Randal L. Schwartz, Brian D Foy, Tom Phoenix ; **ISBN-13:** 978-1-4493-0358-7 ASU Lib
- *Intermediate Perl* (1st Edition), **Author:** Randal L. Schwartz; Brian D Foy; Tom Phoenix ; **ISBN-13:** 978-1-4493-9309-0 ASU Lib

¹If you are buying this as a reference you should purchase the second edition

- *Digital Design and Computer Architecture: From Gates to Processors* **Author:** Harris, David Money ; Harris, Sarah L. **ISBN-13** 978-0-1237-0497-9 ASU Lib
- ASIC World – Some tutorials and description of SystemVerilog
- Stack Exchange – A question and answer site that may have answers to some of your questions
- Makefile tutorial
- Linux tutorial
- EDA Playground – An online interactive IDE for SystemVerilog.
- Genesis2 – A guide to the generator you may use in class.