

EEE 333 Hardware Design Languages and Programmable Logic (4) [Fall, Spring]

Course (Catalog) Description:

Develops digital logic with modern practices of hardware description languages. Emphasizes usage, synthesis of digital systems for programmable logic, VLSI.
Lecture, laboratory.

Course Type: Required for majors in bioengineering, computer systems engineering, and electrical engineering.

Prerequisite: CSE 120 or EEE 120, EEE 202

Textbook: *The Designer's Guide to VHDL*, by Peter J. Ashenden, 3rd Ed, Morgan Kaufmann Publishers, 2008, ISBN: 9780120887859

Supplemental Materials: Instructor notes available from course websites (Blackboard LMS), Xilinx CPLD and FPGA design notes, Xilinx FPGA design software (Xilinx ISE with Modelsim or iSim), Digilent FPGA boards.

Coordinator: TBD

Course Objective:

1. Students can design digital circuits using a hardware description language and synthesis.
2. Students understand modern programmable logic devices and can use them in practical applications.
3. Students understand timing and effects of hardware mapping and circuit parasitics.

Course Outcomes:

1. Students can apply logic fundamentals using hardware description languages.
2. Students understand the difference between procedural programming and hardware description languages.
3. Students can write synthesizable verilog code describing basic logic elements
 - a. Combinatorial logic.
 - b. Sequential logic.
4. Students can code state machines in a hardware description language.
5. Students can analyze and develop basic logic pipelined machines.
6. Students understand basic programmable logic architectures.
7. Students can synthesize working circuits using programmable logic.
8. Students understand sequential and combinatorial logic timing.
9. Students understand the impact of actual routing and circuit parasitics.

Course Topics:

1. Review logic fundamentals, gates, latches, flip-flops and state machines (2 weeks).
2. Verilog HDL fundamentals, simulation, and test-bench design (4 weeks).
3. Synthesizable code and hardware/HDL mapping (3 weeks).
 - a. Basic logic.

- b. Sequential circuits.
- c. Arithmetic circuits.
- 4. CPLD architecture and synthesis (3 weeks).
- 5. FPGA architecture and synthesis (4 weeks).

Computer Usage:

Modelsim or iSim and FPGA synthesis tools..

Laboratory Experiments:

Students meet weekly for a three-hour laboratory under the guidance of a TA.

Course Contribution to Engineering Science and Design:

EEE 333 contributes to engineering science through logic design, problem solving, and computer solutions.

Course Relationship to Program Objectives:

This course is a detailed introduction to a hardware description language (HDL), for example VHDL or Verilog for contemporary design of ASIC and FPGA systems. The material covers CMOS digital logic, VHDL coding and modeling, synthesis and verification, and FPGA design basics (c,k). The comprehensive lectures will address the knowledge of a hardware-oriented HDL primer, such as HDL data types, testbenches, Finite State Machines (FSMs), and memory structures (e,k). The fundamental learning will be reinforced by realistic examples for each topic and by practical lab exercises (b,c). Laboratory teams feature various engineering majors (d). The knowledge gained in this course can be applied to any VLSI design by using a top-down design methodology (e).

3(b): Significant laboratory experience.

3(c): Significant design.

3(d): Laboratory teams feature various engineering majors.

3(e): Students are solving engineering problems.

3(k): Modelsim/iSim and FPGA synthesis software is used.

Person preparing this description and date of preparation: Michael Goryll, May. 2015.