ABSTRACT

Accessibility to the internal nodes of an analog/mixed-signal circuit while testing is extremely difficult. Furthermore, with technology scaling, the effect of process variations becomes more pronounced. This tends to affect the test time, test cost and die yield. As devices become more unreliable, the probability of failure of a die increases, thus decreasing the yield. This, in turn, increases the test cost and decreases the quality of test. Therefore, test time minimization and test cost reduction are important. Moreover, process variations can affect the performance of analog/mixed circuits. Therefore, the performance of a SoC which tends to integrate multiple band gap reference circuits (BGRs) is effected due to the wide variations caused in the behavior of the BGR as a result of increasing process variations. Calibration of the BGR is, thus, important in the test process so as to obtain accuracy in the measurement of the output voltage of BGR. Furthermore, as test time minimization and test cost reduction are important in a test process, Built-in Self Test (BIST) techniques have become more popular. This led to the design of a VCO-based zoom-in ADC architecture that was built to calibrate the output of the BGR voltage which dictates the circuit performance. However, the zoom-voltages for the circuit are generated using a tester. As the number of such ADCs integrated on a SoC increase, the number of nodes to be accessed by the tester increase. Therefore, accessibility decreases with increase in scaling. Moreover, the capacitance of the probe affecting the accuracy of applying the voltages to the input of the VCO-based ADC increases with scaling. Further, generating a wide range of inputs becomes burdensome for the tester. For all the above reasons, an on-chip DAC circuitry was proposed as a part of this thesis, to decrease the reliance on tester. The suggested DAC architecture is a simple resistor string whose resolution depends on the number of zoom-in voltages to be generated. This architecture has a linear and monotonic behavior which is very important as the VCO has a highly non-linear behavior. Thus, the voltages generated by the DAC should be accurate with minimum error so that
the worst-case INL is less than 1mV considering resistor mismatches over process variations. With the increase in the number of VCO-based ADCs on a chip, the test time savings increase exponentially. Thus, the introduction of on-chip DAC circuitry offers various advantages like decreasing accessibility requirement during test, occupying less area, test cost savings and most importantly, decreasing the reliance on tester.