

EEE 598: Neuromorphic Computing Hardware Design (Spring 2017)

Class hours:

Tue. & Thu. 4:30pm-5:45pm, Wexler Hall A203

Instructor:

Prof. Jae-sun Seo (jaesun.seo@asu.edu), ISTB4 551B

Pre-requisite:

- Comfortable with Matlab, Python or similar languages for algorithm development
- EEE 525 or equivalent
- Experienced with RTL coding, synthesis, and automatic place and route (APR)

Course description: In recent years, both industry and academia have shown large interest in low-power hardware designs for neuromorphic computing (e.g. TrueNorth) and deep learning algorithms (e.g. convolutional neural networks) for a wide range of image, speech, and biomedical applications. In this course, we will learn the underlying theory, basic algorithms, and efficient device/circuit/architecture design of neuromorphic computing.

Course topics:

- Computation in the brain and related learning algorithms
- Biological neuron models and implementations
- Biological synapse models and implementations
- Analog vs. digital design of neuromorphic hardware
- Device-level design techniques for neuromorphic computing
- Circuit-level design techniques for neuromorphic computing
- Architecture-level design techniques for neuromorphic computing
- Case studies of large-scale neuromorphic hardware implementations

Homework: The homework assignments will be posted on the class website. Late submissions will not be allowed. Students may work together on the homework, but copying is unacceptable.

Laboratory: The laboratory is located in GWC 273. There will be several laboratory assignments (learning algorithm design, custom digital CMOS hardware design) which will cover algorithm, circuit and architecture design using EDA tools (Cadence, Synopsys, etc.) using a given CMOS technology. Details of the laboratory assignments, due dates, etc. will be posted on the class website.