Mohsen Imani

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Research Interests

- Brain-Inspired Computing, Neuromorphic Computing, Machine Learning
- Computer Architecture, Non-von Neumann Architecture, Processing in Memory
- Embedded Systems, Energy-Efficient Systems, Internet of Things, HW/SW Co-design

Education

2014–Present **PhD Candidate**, *University of California San Diego*, La Jolla, CA, USA.
Computer Science and Engineering
Thesis Title: Towards Learning with Brain Efficiency

2011–2014 **Master of Science**, *University of Tehran*, Tehran, IR.
Electrical and Computer Engineering

2007–2011 **Bachelor of Science**, *University of Tehran*, Tehran, IR.
Electrical and Computer Engineering

Publication Summary

- Google Scholar Summary (as of 11/01/2019): **Citations: 1,314, *h-index*: 22, *i10-index*: 38** (Link).
- **Selected publications**:

1. **M. Imani**, A. Rahimi, D. Kong, T. Rosing, J. M. Rabaey, "Exploring Hyperdimensional Associative Memory", *International Symposium on High-Performance Computer Architecture (HPCA)*, 2017.
2. **M. Imani**, S.Gupta, Y. Kim, T. Rosing, "FloatPIM: In-Memory Acceleration of Deep Neural Network Training with High Precision", *IEEE International Symposium on Computer Architecture (ISCA)*, 2019.
3. **M. Imani**, Y. Kim, M. S. Riazi, J.Messerly, P. Liu, F. Koushanfar, T. Rosing, "A Framework for Collaborative Learning in Secure High-Dimensional Space", *IEEE Cloud Computing (CLOUD)*, 2019.
4. **M. Imani**, M. Samragh, Y. Kim, S. Gupta, F. Koushanfar, T. Rosing, "Deep Learning Acceleration with Neuron-to-Memory Transformation", IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2020.

Awards and Honors

2019 **Bernard and Sophia Gordon Engineering Leadership Award ($\$10,000$)**, the most prestigious leadership award in the school of engineering, UC San Diego.

2019 **Best Paper Candidate**, at Design Automation Conference (DAC), Las Vegas, NV.

2019 **Outstanding Jacobs School of Engineering Graduate Research Award**, recognized as an exceptional graduate student contributed to several funded grants and minorities research programs at UC San Diego.

2019 **Best Poster/Presentation Award** (Ranked 1st), PhD Forum, Design Automation Conference (DAC), Las Vegas, NV.

2019 **Best Presentation Award**, SRC Techcon Conference, Austin, TX.

2018 **Best Doctoral Research Award**, Computer Science Department, UC San Diego.

2018 **Best Poster Award**, Research Expo, San Diego, CA.

2018 **Best paper Candidate**, at International Symposium on Quality Electronic Design (ISQED), CA

2014-2017 **Powell-Focht Fellowship**, the prestigious three-years full scholarship at UC San Diego.

2016 **Best Paper Candidate**, at International Conference on Computer Design (ICCD), Phoenix, AZ.

2016-2019 **NSF Travel Grant Award**, at multiple confences including ISCA 2019, DAC 2019, BHI 2019, BHI 2018, and GLSLVSI 2016.

2015 **Young Richard Newton Student Fellow**, at Design Automation Conference (DAC).

2014 **Best Teaching Assistant Award**, University of Tehran, Tehran, IR.

2011 **Ranked 9th** among more than 40,000 participants in Iranian Nationwide University Entrance Exam for M.Sc. degree in Electrical Engineering.

2007 **Ranked 81st** among more than 400,000 participants in Iranian Nationwide University Entrance Exam for B.Sc. degree.

Publications

Book Chapter:

[B1] **M. Imani**, T. Rosing, "Approximate CPU and GPU Design Using Emerging Memory Technologies", *Springer's book titled Approximate Circuit*, 2019.

Conferences:

[C45] **M. Imani**, M. Samragh, Y. Kim, S. Gupta, F. Koushanfar, T. Rosing, "Deep Learning Acceleration with Neuron-to-Memory Transformation", IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2020 (acceptance rate 19.3%).

[C44] **M. Imani**, S.Gupta, Y. Kim, T. Rosing, "FloatPIM: In-Memory Acceleration of Deep Neural Network Training with High Precision", *IEEE International Symposium on Computer Architecture (ISCA)*, 2019 (acceptance rate 16.9%).

[C43] **M. Imani**, Y. Kim, M. S. Riazi, J.Messerly, P. Liu, F. Koushanfar, T. Rosing, "A Framework for Collaborative Learning in Secure High-Dimensional Space", *IEEE Cloud Computing (CLOUD)*, 2019 (acceptance rate 14.3%).

[C42] **M. Imani**, S. Bosch, M. Javaheripi, B. Rouhani, X. Wu, F. Koushanfar, T. Rosing, "SemiHD: Semi-Supervised Learning Using Hyperdimensional Computing", *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2019.

[C41] S. Salamat, B. Khaleghi, **M. Imani**, T. Rosing, "Workload-Aware Opportunistic Energy Efficiency in Multi-FPGA Platforms", *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2019.

[C40] **M. Imani**, S. Salamat, B. Khaleghi, M. Samragh, F. Koushanfar, T. Rosing, "SparseHD: Algorithm-Hardware Co-Optimization for Efficient High-Dimensional Computing", *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2019.

[C39] **M. Imani**, J. Morris, J. Messerly, H. Shu, Y. Deng, T. Rosing, "BRIC: Locality-based Encoding for Energy-Efficient Brain-Inspired Hyperdimensional Computing", *IEEE/ACM Design Automation Conference (DAC)*, 2019. (Best Paper Candidate)

[C38] **M. Imani**, a. Sokolova, R. Garcia, A. Huang, F. Wu, B. Aksanli, T. Rosing, "ApproxLP: Approximate Multiplication with Linearization and Iterative Error Control", *IEEE/ACM Design Automation Conference (DAC)*, 2019.

[C37] D. Peroni, **M. Imani**, H. Nejatollahi, N, Dutt, T. Rosing, "ARGA: Approximate Reuse for GPGPU Acceleration", *IEEE/ACM Design Automation Conference (DAC)*, 2019.

[C36] M. Zhou, **M. Imani**, S. Gupta, T. Rosing, "Thermal-Aware Design and Management for Search-based In-Memory Acceleration", *IEEE/ACM Design Automation Conference (DAC)*, 2019.

[C35] S. Salamat, **M. Imani**,B. Khaleghi, T. Rosing, "F5-HD: Fast Flexible FPGA-based Framework for Refreshing Hyperdimensional Computing", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, 2019.

[C34] **M. Imani**, J.Messerly, F. Wu, W. Pi, T. Rosing, "A Binary Learning Framework for Hyperdimensional Computing", *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2019.

[C33] **M. Imani**, Y. Kim, T. Worley, S. Gupta, T. Rosing, "HDCluster: An Accurate Clustering Using Brain-Inspired High-Dimensional Computing", *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2019.

[C32] **M. Imani**, R. Garcia, A. Huang, T. Rosing, "CADE: Configurable Approximate Divider for Energy Efficiency", *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2019.

[C31] **M. Imani**, J. Morris, S. Bosch, H. Shu, G. De Micheli, T. Rosing, "AdaptHD: Adaptive Efficient Training for Brain-Inspired Hyperdimensional Computing", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2019.

[C30] S.Gupta, **M. Imani**, B.Khaleghi, V.Kumar, T.Rosing, "RAPID: A ReRAM Processing in Memory Architecture for DNA Sequence Alignment", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2019.

[C29] J.Morris, **M. Imani**, S.Bosch, A.Thomas, H.Shu, T.Rosing"CompHD: Efficient Hyperdimensional Computing Using Model Compression", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2019.

[C28] Y. Kim, **M. Imani**, T. Rosing, "Efficient Human Activity Recognition Using Hyperdimensional Computing", *IEEE Conference on Internet of Things (IoT)*, 2019.

[C27] **M. Imani**, S. Salamat, J. Huang, S. Gupta, T. Rosing, "FACH: FPGA-based Acceleration of Hyperdimensional Computing by Reducing Computational Complexity", *IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2019.

[C26] M. Zhou, **M. Imani**, S. Gupta, Y. Kim, T. Rosing, "GRAM: Graph Processing in a ReRAM-based Computational Memory", *IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2019.

[C25] D. Peroni, **M. Imani**, T. Rosing, "ALook: Adaptive Lookup for GPGPU Acceleration", *IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2019.

[C24] S. Gupta, **M. Imani**, T. Rosing, "FELIX: Fast and Energy-Efficient Logic in Memory", *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2018.

[C23] **M. Imani**, Y. Kim, T. Rosing, "Brain-Inspired Hyperdimensional Computing: An Efficient Classifier for Embedded Devices", *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2018.

[C22] **M. Imani**, R. Garcia, S. Gupta, T. Rosing, "RMAC: Runtime Configurable Floating Point Multiplier for Approximate Computing", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2018.

[C21] M. Zhou, **M. Imani**, S. Gupta, T. Rosing, "GAS: A Heterogeneous Memory Acceleration for Graph Processing", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2018.

[C20] **M. Imani**, S. Gupta, S. Sharma, T. Rosing, "Hierarchical Hyperdimensional Computing for Energy Efficient Classification", *IEEE/ACM Design Automation Conference (DAC)*, 2018.

[C19] **M. Imani**, R. Garcia, S. Gupta, T. Rosing, "Configurable Floating Point Multiplier for Approximate Computing", *IEEE/ACM Design Automation Conference (DAC)*, 2018.

[C18] S. Gupta, **M. Imani**, T. Rosing, "Processing In-Memory Architecture for Multiple Memory Technology", *IEEE/ACM Design Automation Conference (DAC)*, 2018.

[C17] **M. Imani**, S. Gupta, T. Rosing, "GenPIM: Generalized Processing In-Memory to Accelerate Data Intensive Applications", *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2018.

[C16] J. sim, **M. Imani**, Y. Kim, W. Choi, T. Rosing, "LUPIS : Latch-Up Based Ultra Efficient Processing In-Memory System", *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2018. (Best Paper Candidate)

[C15] **M. Imani**, M. Masich, D. Peroni, P. Wang, T. Rosing, "CANNA: Neural Network Acceleration using Configurable Approximation on GPGPU", *IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2018.

[C14] **M. Imani**, A. Rahimi, D. Kong, T. Rosing, J. M. Rabaey, "Exploring Hyperdimensional Associative Memory", *International Symposium on High-Performance Computer Architecture (HPCA)*, 2017 (acceptance rate 22%).

[C13] **M. Imani**, S. Gupta, T. Rosing, "Ultra-Efficient Processing In-Memory for Data Intensive Applications", *IEEE/ACM Design Automation Conference (DAC)*, 2017.

[C12] **M. Imani**, D. Peroni, D. Kong, T. Rosing, "CFPU: Configurable Floating Point Multiplier for Energy-Efficient Computing", *IEEE/ACM Design Automation Conference (DAC)*, 2017 (Best Poster Award at Research Expo).

[C11] Y. Kim, **M. Imani**, T. Rosing, "ORCHARD: Visual Object Recognition Accelerator Based on Approximate In-Memory Processing", *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2017.

[C10] **M. Imani**, D. Peroni, Y. Kim, A. Rahimi, T. Rosing, "Efficient Neural Network Acceleration on GPGPU using Content Addressable Memory," *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2017.

[C9] M. Samragh, **M. Imani**, F. Koushanfar, T. Rosing, "LookNN: Neural Network with No Multiplication," *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2017.

[C8] **M. Imani**, S. Gupta, A. Arredondo, T. Rosing, "Efficient Query Processing in Crossbar Memory", *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2017.

[C7] **M. Imani**, Y. Kim, T. Rosing, "MPIM: Multi-Purpose In-Memory Processing using Configurable Resistive Memory", *IEEE Asia and South Pacific Design Automation Conference (ASPDAC)*, 2017.

[C6] **M. Imani**, D. Peroni, A. Rahimi, T. Rosing, "Resistive CAM Acceleration for Tunable Approximate Computing", *IEEE International Conference on Computer Design (ICCD)*, 2016. (Best Paper Candidate).

[C5] **M. Imani**, Y. Kim, A. Rahimi, T. Rosing, "Associative Memory with Online Learning for Approximate Computing", Poster presentation in *IEEE/ACM Design Automation Conference (DAC)*, 2016.

[C4] **M. Imani**, Y. Kim, A. Rahimi, T. Rosing, "ACAM: Approximate Computing Based on Adaptive Associative Memory with Online Learning" *International Symposium on Low Power Electronics and Design (ISLPED)*, 2016.

[C3] **M. Imani**, A. Rahimi, T. Rosing, "Resistive Configurable Associative Memory for Approximate Computing," *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2016.

[C2] **M. Imani**, S. Patil, T. Rosing, "MASC: Ultra-Low Energy Multiple-Access Single-Charge TCAM for Approximate Computing," *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, 2016.

[C1] Y. Kim, **M. Imani**, S. Patil, T. Rosing, "CAUSE: Critical Application Usage-Aware Memory System using Non-volatile Memory for Mobile Devices," *IEEE International Conference On Computer Aided Design (ICCAD)*, 2015.

Journals:

[J19] **M. Imani**, S. Bosch, S. Datta, S. Ramakrishna, S. Salamat, J. Rabaey, T. Rosing, "QuantHD: A Quantization Framework for Hyperdimensional Computing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019.

[J18] **M. Imani**, X. Yin, J, Messerly, S. Gupta, M. Nemier, X. S. Hu, T. Rosing, "SearcHD: A Memory-Centric Hyperdimensional Computing with Stochastic Training", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019.

[J17] D. Peroni, **M. Imani**, H. Nejatollahi, N. Dutt, T. Rosing, "Data Reuse for Accelerated Approximate Warps", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019.

[J16] **M. Imani**, A. Morris, H. Shu, S. Li, T. Rosing, "Efficient AssociativeLow-Power Separch in Brain-Inspired Hyperdimensional Computingse Hyperdimensional Encoder for Language Recognition", *IEEE Design & Test (D&T)*, 2019.

[J15] **M. Imani**, R. Garcia, S. Gupta, T. Rosing, "Hardware-Software Co-design to Accelerate Neural Network Applications", *ACM Journal on Emerging Technologies in Computing (JETC)*, 2019.

[J14] D. Peroni, **M. Imani**, T. Rosing, "Runtime Efficiency-Accuracy Trade-off Using Configurable Floating Point Multiplier", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019.

[J13] S. Gupta, **M. Imani**, H. Kaur, T. Rosing, "NNPIM: A Processing In-Memory Architecture for Neural Network", *IEEE Transactions on Computers (TC)*, 2019.

[J12] Y. Kim, **M. Imani**, T. Rosing, "Image Recognition Accelerator Design Using In-Memory Processing", *IEEE Micro, 2018.*

[J11] **M. Imani**, S. Gupta, S. Sharma, T. Rosing, "NVQuery: Efficient Query Processing in Non-Volatile Memory", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2018.

[J10] **M. Imani**, A. Rahimi, J. Hwang, T. Rosing, J. M. Rabaey, "Low-Power Sparse Hyperdimensional Encoder for Language Recognition", *IEEE Design & Test (D&T)*, 2017.

[J9] **M. Imani**, M. Imani, A. Rahimi, P. Mercati, T. Rosing, "Multi-stage Tunable Approximate Search in Resistive Associative Memory," *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*, 2017.

[J8] **M. Imani**, D. Peroni, A. Rahimi, T. Rosing, "Resistive CAM Acceleration for Tunable Approximate Computing", *IEEE Transaction on Emerging Topics in Computing (TETC)*, 2017.

[J7] **M. Imani**, S. Patil, T. Rosing, "Approximate Computing using Multiple-Access Single-Charge Associative Memory", *IEEE Transaction on Emerging Topics in Computing (TETC)*, 2016.

[J6] **M. Imani**, M. Jafari, B. Ebrahimi, T. Rosing, "Ultra-low power FinFET based SRAM cell employing sharing current concept" *Microelectronic Reliability Elsevier Journal*, 2015.

[J5] H. Alimohamadi, **M. Imani**, B. Forouzandeh "Computational Analysis of Transient non-Newtonian Blood Flow in Magnetic Targeting Drug Delivery in Stenosed Carotid Bifurcation Artery," *International Journal of Fluid Mechanics Research, Begell house*, vol. 42, no. 2, pp. 149-169, 2015.

[J4] M. Jafari, **M. Imani**, M. Fathipour, "Analysis of Power Gating in Different Hierarchical Levels of 2MB Caches, Considering Variation," *International Journal of Electronic, Taylor and Francis*, vol. 105, no. 2, pp. 1594-1608, 2014.

[J3] G. Passandi, M. Jafari, **M. Imani**, "A New Low-Power 10T SRAM cell with Improved Read SNM," *International Journal of Electronic, Taylor and Francis*, vol. 105, no. 2, pp. 1621-1633, 2014.

[J2] H. Alimohamadi,**M. Imani**, "Finite Element Simulation of Two-Dimensional Pulsatile Blood Flow thorough a Stenosed Artery in the Presence of External Magnetic Field," *International Journal for Computational Methods in Engineering Science & Mechanics, Taylor and Francis*, vol. 15, no. 4, pp. 390-400, 2014.

[J1] H. Alimohamadi, **M. Imani**, "Transient Non-Newtonian Blood Flow under Magnetic Targeting Drug Delivery in an Aneurysm Blood Vessel with Porous Walls," *International Journal for Computational Methods in Engineering Science & Mechanics, Taylor and Francis*, vol. 15, no. 6, pp. 522-533, 2014.

Other Proceedings & Workshops:

[37] **M. Imani**, S. Gupta, T. Rosing, "A High Precision Processing In-Memory For Deep Learning Acceleration", *SRC Techcon Conference*, 2019. (Best Presentation Award).

[36] **M. Imani**, S. Gupta, T. Rosing, "Digital-based Processing In-Memory: A Highly-Parallel Accelerator for Data Intensive Applications", *ACM International Symposium on Memory Systems (MEMSYS)*, 2019.

[35] **M. Imani**, S. Gupta, Y. Kim, M. Zhou, T. Rosing, "DigitalPIM: Digital-based Processing In-Memory for Big Data Acceleration", *ACM Great lakes symposium on VLSI (GLSVLSI)*, 2019. (**Invited Talk**)

[34] J. Sim, S. Gupta, **M. Imani**, Y. Kim, T. Rosing, "UPIM : Unipolar Switching Logic for High Density Processing-in-Memory Applications", *ACM Great lakes symposium on VLSI (GLSVLSI)*, 2019.

[33] S. Gupta, **M. Imani**, T. Rosing, "Exploring Processing In-Memory for Different Technologies", *ACM Great lakes symposium on VLSI (GLSVLSI)*, 2019.

[32] **M. Imani**, T. Nassar, A. Rahimi, T. Rosing, "Brain-Inspired Hyperdimensional Computing for Real-Time Health Analysis" *IEEE International Conference on Biomedical and Health Informatics (BHI)*, 2019.

[31] **M. Imani**, D. Peroni, T. Rosing, "Program Acceleration Using Nearest Distance Associative Search", *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2018.

[30] **M. Imani**, D. Kong, A. Rahimi, T. Rosing, "VoiceHD: Hyperdimensional Computing for Efficient Speech Recognition", *IEEE International Conference on Rebooting Computing (ICRC)*, 2017.

[29] **M. Imani**, Y. Kim, T. Rosing, "NNgine: Ultra-Efficient Nearest Neighbor Accelerator Based on In-Memory Computing", *IEEE International Conference on Rebooting Computing (ICRC)*, 2017.

[28] **M. Imani**, S. Patil, T. Rosing, "Hierarchical Design of Robust and Low Data Dependent 32KB FinFET Based SRAM Array," *IEEE International Symposium on Nanoscale Architecture (NANOARCH)*, 2015.

[27] **M. Imani**, T. Nassar, A. Rahimi, T. Rosing, "HDNA: Energy-Efficient DNA Sequencing Using Hyperdimensional Computing", *IEEE International Conference on Biomedical and Health Informatics (BHI)*, 2018.

[26] **M. Imani**, Y. Kim, S. Gupta, D. Peroni, T. Rosing, "In-Memory Acceleration of Deep Neural Network", *GOMACTech Conference, 2019.*

[25] **M. Imani**, M. Samragh, Y. Kim, S.Gupta, F. Koushanfar, T. Rosing, "A Fully Digital In-Memory Acceleration of Deep Neural Network", Non-Volatile Memory Workshop (NVMW), 2019.

[24] J. Sim, **M. Imani**, W. Choi, Y. Kim, T. Rosing, "Current-Sensing Efficient Adder for Processing-in-Memory Design", Non-Volatile Memory Workshop (NVMW), 2019.

[23] **M. Imani**, T. Nassar, J. Morris, T. Rosing, "DNA Sequencing using Brain-inspired Hyperdimensional Computing", *GOMACTech Conference, 2019.*

[22] **M. Imani**, T. Nassar, T. Rosing, "Moving Toward Real-Time Diagnostics using Brain-Inspired Hyperdimensional Computing", *AACR conference on Artificial Intelligence, Big Data, and Prediction in Cancer*, 2018.

[21] **M. Imani**, D. Peroni, T. Rosing, "Resistive Content Addressable Memory for Configurable Approximation", *GOMACTech conference*, 2018.

[20] **M. Imani**, M. Masich, T. Rosing, "Training Acceleration of Deep Neural Network on Configurable GPGPU", Techon SRC Conference, 2018.

[19] **M. Imani**, . Kim, T. Rosing, "Hyperdimensional Computing: A Light-Weight Cognitive Machine" White Paper NSF IoT Workshop, 2018 .

[18] **M. Imani**, . Kim, T. Rosing, "Visual Object Recognition Accelerator Based on Approximate In-Memory Processing", Non-Volatile Memory Workshop (NVMW), 2018 .

[17] **M. Imani**, A. Rahimi, D. Kong, T. Rosing, Jan Rabaey, "Non-Volatile Associative Memory to Accelerate Brain-inspired Hyperdimensional Computing", Non-Volatile Memory Workshop (NVMW), 2018.

[16] S. Salamat, **M. Imani**, S. Gupta, T. Rosing, "RNSnet: In-Memory Neural Network Acceleration Using Residue Number System", *IEEE International Conference on Rebooting Computing (ICRC)*, 2018.

[15] T. Kim, **M. Imani**, T. Rosing, "General-Purpose Online Classification Accelerator via In-Memory Computing", *Techon SRC Conference*, 2017.

[14] **M. Imani**, A. Rahimi, D. Kong, T. Rosing, J. M. Rabaey, "Hardware Acceleration of Brain-inspired Hyperdimensional Computing", *IEEE/ACM ICCAD, Workshop on Variability, Modeling, and Characterization (VMC)*, 2017.

[13] **M. Imani**, Y. Cheng, T. Rosing, "Processing Acceleration with Resistive Memory-based Computation," *ACM International Symposium on Memory Systems (MEMSYS)*, 2016.

[12] **M. Imani**, P. Mercati, T. Rosing, "ReMAM: Low Energy Resistive Multi-Stage Associative Memory for Energy

Efficient Computing," *International Symposium on Quality Electronic Design (ISQED)*, 2016.

[11] **M. Imani**, S. Patil, T. Rosing, "Low Power Data-Aware STT-RAM based Hybrid Cache Architecture," *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2016.

[10] P. Mercati, A. Bartolini, F. Paterna, **M. Imani**, L. Benini and T. Rosing, "VarDroid: Online Variability Emulation in Android/Linux Platforms," *ACM Great lakes symposium on VLSI (GLSVLSI)*, 2016.

[9] **M. Imani**, S. Patil, T. Rosing, "DCC: Double Capacity Cache for Narrow-Width Data Values," *ACM Great lakes symposium on VLSI (GLSVLSI)*, 2016.

[8] **M. Imani**, S. Patil, M. Jafari, T. Rosing, "Ultra-Low Read leakage SRAM Cell Utilizing Independently-Controlled-Gate FinFET," Poster in *IEEE/ACM Design Automation Conference (DAC)*, 2015.

[7] **M. Imani**, A. Rahimi, Y. Kim, T. Rosing, "A Low-Power Hybrid Magnetic Cache Architecture Exploiting Narrow-Width Values," *Non-Volatile Memory Systems and Applications Symposium (NVMSA)*, 2016.

[6] **M. Imani**, M. Imani, Y. Kim, A. Rahimi, T. Rosing, "In-Memory Processing to Support Search-Based and Bitwise Computation", *Non-Volatile Memory Workshop (NVMW)*, 2017.

[5] **M. Imani**,D. Peroni, A. Rahimi, T. Rosing, "Non-volatile Content Addressable Memory for Computing Acceleration", *Non-Volatile Memory Workshop (NVMW)*, 2017.

[4] **M. Imani**, Y. Kim, T. Rosing, "In-Memory Processing to Support Search-Based and Bitwise Computation", *Non-Volatile Memory Workshop (NVMW)*, 2017.

[3] **M. Imani**, B. Aksanli, T. Rosing, "Ultra-Efficient Content Addressable Memory for Tunable GPU Approximation," *Techon SRC Conference*, 2016.

[2] **M. Imani**, S. Patil, T. Rosing, "Using STT-RAM Based Buffers in Digital Circuits," *Annual Non-Volatile Memories Workshop*, 2015.

[1] **M. Imani**, Y. Cheng, T. Rosing, "Resistive Memory for Approximate Program Acceleration", *Annual Non-Volatile Memories Workshop*, 2015.

Under Review:

[ISCA] **M. Imani**, S. Bosch, Y. Kim, S. Rao, S. Salamat, V. Kumar, T. Rosing, "Revisiting Brain-Inspired Hyperdimensional Computing for Low-Power Architectures", *Under Review* in the *IEEE International Symposium on Computer Architecture (ISCA)*, 2020.

[ISCA] **M. Imani**, S. Pampana, S. Gupta, Y. Kim, M. Zhou, T. Rosing, "DUAL: Acceleration of Unsupervised Learning using Digital-based Processing In-Memory", *Under Review* in the *IEEE International Symposium on Computer Architecture (ISCA)*, 2020.

[ISCA] Y. Kim, **M. Imani**, S. Gupta, T. Rosing, "Hyperdimensional Processing System: An Efficient Cognitive Machine", *Under Review* in the *IEEE International Symposium on Computer Architecture (ISCA)*, 2020.

[TCAD] A. Sokolova, **M. Imani**, A. Huang, R. Garcia, J. Morris, T. Rosing, B. Aksanli, "MACcelerator: Approximate Arithmetic Unit for Computational Acceleration", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019.

[TCAS] S. Salamat, **M. Imani**, T. Rosing, "HD-Core: Exploiting Computational Reuse for FPGA-based Acceleration of Hyperdimensional Computing", *IEEE Transactions on Circuits and Systems I (TCAS I), 2019.*

Contribution on Funded Grants

The impact of my Ph.D. contribution on governmental agencies:

- Convinced National Science Foundation (NSF) to put HyperDimensional computing in NSF 2019 call for proposal.
- Convinced Semiconductor Research Cooperation (SRC) to put HyperDimensional computing beside Artificial Intelligence research in the SRC 2019 call for proposal.
- DARPA released a new call for proposal, called "*Hyper-Dimensional Data Enabled Neural Networks (HyDDENN)*", which is entirely based on my Ph.D. research– as it has been referenced in the proposal (Link).

Actively contributed on four successful proposal grants funded by the NSF, three grants funded by SRC, and multiple grants from Intel, IBM, ARM, Sony, Samsung, Qualcomm, and DARPA. Examples are listed below:

- **SRC JUMP CRISP:** A Center for Research on Intelligent Storage and Processing-in-memory, supported by DARPA and semiconductor Research Corporation (Awarded Amount: $40M Grants).
- **SRC Team Grant:** An extra grant as a part of JUMP, Title: Automated Task Scheduling for Programmable Processing-in-Memory Systems (Awarded Amount: $200,000 Grants).
- **SRC-Intel Grant:** Brain-inspired Hyper-Dimensional Computing Based on Processing In-Memory (Awarded

Amount: $300,000 Grants).

- **NSF #1911095**: FET: Brain-Inspired Hyperdimensional Computing for IoT Applications (Awarded Amount: $500,000).
- **NSF #1527034**: ENACT: Environment-Aware Management of Mobile Systems (Awarded Amount: $466,000).
- **NSF #1826967**: NPEO: Toward the National Research Platform (Awarded Amount: $2,516,000).
- **NSF #1730158:** Cognitive Hardware and Software Ecosystem Community Intrastructure (Awarded Amount: $1,199,998).
- **NSF REU:** Multiple Research Experiences for Undergraduates grants based on NSF #1527034 and NSF #1730158.

Teaching Experience

PRIMARY INSTRUCTOR:

Spring 2018 **CSE 291: Alternative Computing Paradigm** , *UC San Diego, CSE Department*.
Co-teaching with Prof. Tajana Rosing at UC San Diego.

Summer 2017 **CSE 140*: Components and Design Techniques for Digital Systems**, *UC San Diego, CSE Department*.

Summer 2017 **CSE 140L*: Digital Systems Laboratory**, *UC San Diego, CSE Department*..
* Strongly recommended by 98.1% of students in the post-class instructor evaluation, which put me among the most popular computer science instructors at UC San Diego

TEACHING ASSISTANT:

Fall 2015 **Digital Logic Design**, *UC San Diego, CSE Department*.
Instructor: Prof. Tajana Rosing

2012, 2013 **Communications Circuits**, *University of Tehran, ECE Department*.
Instructor: prof. Mahmud Kamarei

2013, 2014 **MEMS & NEMS**, *University of Tehran, ECE Department*.
Instructor: Prof. Morteza Fathipur

2012, 2014 **Electronic Circuits I**, *University of Tehran, ECE Department*.
Instructor: Prof. Mohammadreza Kolahdouz

2010, 2014 **Electronic Circuit II**, *University of Tehran, ECE Department*.
Instructor: Prof. Behjat Frouzandeh

2011 **Basic Electrical I**, *University of Tehran, ME Department*.
Instructor: Prof. Moosa Ayati

2013, 2014 **Basic Electrical II**, *University of Tehran, ME Department*.
Instructor: Prof. Heydar Ramezani-tabar

2012 **Linear Control Systems**, *University of Tehran, ME Department*.
Instructor: Prof. Aghil Yousefi-Koma

Mentorship

Mentored more than 22 undergraduate and 20 graduate students, including 8 PhD students.
Up-to-date list of mentored students: `http://moimani.weebly.com/mentorship.html`

Thesis Mentored:

- **Dr. Daniel Peroni**, Ph.D. CSE, UCSD, Title: Computational Resuse for GPU Approximation, 2019
- **Dr. Joonseop Sim**, Ph.D. ECE, UCSD, Title: Processing In-Memory using Emerging Technology, 2019
- **Saransh Gupta**, MS ECE UCSD, Title: Enabling Efficient In-Memory Processing, 2018
- **Daniel Peroni**, MS CSE, UCSD, Title: Configurable Approximate Computing, 2017
- **Max Masich**, MS CSE, UCSD, Title: Deep Neural Network Acceleration Under the Hardware Uncertainty, 2017

PhD Students:

- **Dr. Daniel Peroni**, CSE PhD, Project: GPU acceleration and approxiamte computing
- **Dr. Joonseop Sim**, ECE PhD, Project: Emerging memory/circuit design

- **Sahand Salamat**, CSE PhD, Project: FPGA acceleration of machine learning algorithms
- **Saransh Gupta**, CSE PhD, Project: Processing in-memory
- **Minxuan Zhou**, CSE PhD, Project: Graph processing
- **Yunhui Guo**, CSE PhD, Project: Deep learning and brain-inspired computing
- **Alice A Sokolova**, ECE PhD, Project: Approximate computing
- **Justin Morris**, ECE PhD, Project: Energy-efficient cognitive machine

Master Students:

- **Sharadhi Ramakrishna**, CSE, Project: FPGA acceleration
- **Sanjay Anantha Rao**, CSE, Project: FPGA acceleration
- **Saikishan Pampana**, CSE, Project: Hierarchical clustering
- **Samuel Bosch**, EPFL, Project: light-weight classification
- **ALUMINA**: **Pushen Wang** (Software engineer at Amazon Inc.), **Harveen Kaur** (Software engineer at Apple Inc.), **Chenyu Huang** (Whitepages, Inc.) , **Sahil Sharma** (Graduate student at UC San Diego), **Max Masich** (Software engineer at Health Company), **Debanjan Chatterjee** (Engineer at Citadel Information Services Inc.), **Chunchun Xu** (Software Development Engineer at Facebook Inc.)

Undergraduate Students:

- **Helen Shu**, CSE, Project: Machine learning acceleration
- **Patrick Liu**, CSE, Project: Data compression in learning
- **Yaobang Deng**, CSE, Project: Object detection
- **Conner Leonard**, CSE, Project: Supervised learning
- **Xinyu Wu**, CSE, Project: Self learning
- **Ricardo Garcia**, ECE, Project: GPU approximation
- **Andrew Huang**, CSE, Project: Approximate arithmetic
- **Jimin Mun**, CSE, Project: Approximate computing
- **ALUMINA**: **Tarek Nassar** (Engineer at Intel Inc.), **Shuo Li** (Graduate Program at Carnegie Mellon University), **Jiani Huang** (Ph.D. student at University of Pennsylvania), **Deqian Kong** (Software engineer at Amazon Inc.), **Atl Arredondo** (Data science engineer at slack Inc.), **Yan Cheng** (Graduate student at CSE, UCSD), **John F Hwang** (Engineer at Parsons Corporation Inc.), **Seven Wu** (Graduate student at University of Chicago), **John P Messerly** (Graduate student at UCSD), **Thomas Worley** (Graduate student at UCSD)

Diversity

Volunteered to participate in several programs aiming to support undergraduate and minority research.

- **ERSP**: a team-based research experience for undergraduate students early in their engineering career.
  - **2018-2019** Roshan Fernando and Leyi Shang, Project: Brain-inspired computing
  - **2017-2018** Joyaan Bhesania, Valeria Gonzalez, Robert Chang-koepp, and Helen Shu, Project: Adaptive learning in high-dimensional space
- **ENLANCE**: a bi-national summer research program at tries to encourage the participation of high school and college students in research, while promoting cross-border friendships in the Baja California/San Diego.
  - **2019** Alejandro Hérnandez, Project: Semi-Supervised Learning
  - **2018** Adrian Chouza and Sebastian Silva, Project: Fast and efficient classification
  - **2017** Angel Torres mota, Claudia Lopez (High school students), Project: A line detection robots

Collaborators

My research opened collaboration with several schools and industries listed below:

Academia:

- UC San Diego (Prof. Farinaz Koushanfar, Prof. Rob Knight, Dr. Jishen Zhao, Dr. Niema Moshiri, Prof. Thomas Defanti), UC Berkeley (Prof. Jan Rabaey), UC Irvine (Prof. Nikil Dutt), EPFL (Prof. Giovanni De Micheli), University of Notre Dame (Prof. Xiaobo Sharon Hu and Prof. Michael Niemier), MIT (Prof. Tomaso Poggio), ETH (Prof. Luca Benini), University of Virginia (Dr. Samira Khan).

Industries:

- AMD, Intel, IBM, ARM, Qualcomm, Samsung, Sony, SK hynix, DARPA.

Talks

Invited Talks

Nov. 2019 Invited talk at Duke University, Host: Prof. krishnendu chakrabarty and Prof. Helen Li.
Nov. 2019 Invited talk at University of California Davis, Host: Prof. S. J. Ben Yoo.
Nov. 2019 Invited talk at University of California Santa Barbara, Host: Prof. Tim Sherwood.
Nov. 2019 Invited talk at University of Colorado, Boulder, Host: Prof. Ashutosh Trivedi.
Oct. 2019 Invited talk at Princeton University, Host: Prof. Niraj K. Jha.
Oct. 2019 Invited talk at Rutgers University, Host: Prof. Yingying (Jennifer) Chen.
Oct. 2019 Invited talk at University of Pennsylvania, Host: Prof. Linh Phan.
Sept. 2019 Invited talk at University of Maryland, Host: Prof. Rajeev Barua.
Sept. 2019 Invited talk at UC Berkeley, Host: Prof. Jan Rabaey.
Sept. 2019 Invited talk at University of Southern California (USC), Host: Prof. Massoud Pedram.
Sept. 2019 Invited talk at Texax A&M, Host: Prof. Jiang Hu.
Sept. 2019 Invited talk at UT Austin, Host: Prof. Andreas Gerstlauer.
July 2019 Invited talk at The EPFL, Lausanne, Switzerland, Host: Prof. Giovanni De Micheli.
July 2019 Invited talk at The University of British Columbia (UBC), Canada, Host: Prof. Sathish Gopalakrishnan.
July 2019 Invited talk at Arizona State University, Host: Prof.Umit Ogras and Prof. Sarma Vrudhula.
June 2019 Invited talk at Northwestern University, Host: Prof.Gokhan Memik.
June 2019 Visiting and talk at MIT, Host: Prof.Tomasso Poggio, Visit: Prof.Arvind.
June 2019 Invited talk at Brown University, Host: Prof.Sherief Reda and Prof.Iris Bahar.
June 2019 Invited talk at Boston University, Host: Prof.Ajay Joshi and Prof.Ayse Coskun.
June 2019 Invited talk at Northeastern University, Host: Prof.David Kaeli, and Dr.Yanzhi Wang.
May 2019 Invited talk in GLSVLSI 2019, DC, Title: "Processing In-Memory for Learning Acceleration".
April 2018 Invited talk at UC Berkeley Wireless Research Center (BWRC), Berkeley, Host: Prof.Jan Rabaey.
Oct. 2017 Invited talk in San Diego State University (SDSU), San Diego, Host: Dr. Baris Aksanli.

Conference Talks

I have participated in 15 different conferences/workshops and presented over 35 talks.

- ISCA (2019), MICRO (2019), HPCA (2017), DAC (2014, 2015, 2016, 2018, 2019), DATE (2019), ICCAD (2016, 2018, 2019), ISLPED (2016, 2017, 2018, 2019),, GLSVLSI (2016, 2019), FCCM (2019), ISQED (2016, 2017, 2018), ICRC (2017), MEMSYS (2016), NANOARCH (2016), NVMW (2015, 2016. 2017, 2018, 2019), BHI (2018, 2019), TECHCON (2016, 2017, 2018), CNS (2017, 2018).

Service

Program committee in multiple venues and **reviewed over 200 papers** in top-tier journals and conferences.

Session Chair

2019 Session Chair in the 2019 International Symposium on Low Power Electronics and Design (ISLPED).

Program Committee Member

2020 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP).
2019 15th IEEE PRIME Conference, IEEE International Conference on Biomedical & Health Informatics (BHI).
2018 31th IEEE SoCC Conference, 14th IEEE PRIME Conference
2017 30th IEEE SoCC Conference, 13th IEEE PRIME Conference.

IEEE Reviewer

Transactions on Very Large Scale Integration Systems (TVLSI), Transactions on Circuits and Systems I (TCAS I), Transactions on Circuits and Systems II (TCAS II), Transactions on Nanotechnology (TNANO), Transactions on Circuits and Systems for Video Technology (TCSVT), Transactions on Emerging Topics in Computing (TETC), Transactions on Computers (TC), IEEE Micro, IEEE Photonics Journal, IEEE Access.

ACM Reviewer

Journal of Emerging Technologies in Computing Systems (JETC), Transactions on Embedded Computing Systems (TECS), Transactions on Architecture and Code Optimization (TACO).

Elsevier Reviewer

Microelectronic Journal Journal, Integration, the VLSI Journal, Computer Methods and Programs in Biomedicine Journal, Journal Engineering Science and Technology, Computers in Biology and Medicine, Journal of Parallel and Distributed Computing (JPDC).

Taylor & Francis and Wiley

International Journal of Electronic, Brain-Computer Interfaces Journal, Software: Practice and Experience Journal.

Conference External Reviewer

2019 IEEE/ACM Design Automation Conference (DAC), Design, Automation and Test in Europe (DATE).

2018 IEEE/ACM Design Automation Conference (DAC), Design, Automation and Test in Europe (DATE).

2017 IEEE/ACM Design, Automation and Test in Europe (DATE).

Services to UC San Diego

2018-2019 Volunteered as a graduate student to help with faculty interview in CSE department at UC San Diego.

2017-2018 Volunteered to be a part of UC San Diego PhD admission committee.

2018 Volunteered to be a part of UC San Diego Master admission committee.

2016-2019 Volunteered to be a part of undergraduate research program at UC San Diego.

2016-2019 Volunteered to be a part of minorities research at UC San Diego.

References

- **Dr. Tajana Rosing**, Professor, a holder of the Fratamico Endowed Chair, IEEE Fellow
  Department of Computer Science and Engineering, University of California San Diego
  ✉ tajana@ucsd.edu ☎ +1 (858) 822-1516 Homepage
- **Dr. Jan M. Rabaey**, Donald O. Pederson Distinguished Professorship, IEEE Fellow
  Department of Electrical Engineering and Computer Science, University of California Berkeley
  ✉ jan@eecs.berkeley.edu ☎ +1 (510) 642-2328 Homepage
- **Dr. Farinaz Koushanfar**, Professor and Henry Booker Faculty Scholar, IEEE Fellow
  Department of Electrical and Computer Engineering, University of California, San Diego
  ✉ farinaz@ucsd.edu ☎ +1 (858) 246-0251 Homepage
- **Dr. Xiaobo Sharon Hu**, Professor, IEEE Fellow
  Department of Computer Science and Engineering, University of Notre Dame
  ✉ shu@nd.edu ☎ +1 (574) 631-9260 Homepage
- **Dr. Chung-Kuan Cheng**, Distinguished Professor, IEEE Fellow
  Department of Computer Science and Engineering, University of California, San Diego
  ✉ ckcheng@ucsd.edu ☎ +1 (858) 534-6184 Homepage
- **Dr. Ryan Kastner**, Professor
  Department of Computer Science and Engineering, University of California, San Diego
  ✉ kastner@ucsd.edu ☎ +1 (858) 534-8908 Homepage

Personal

Residency: U.S. Permanent Resident.

UNIVERSITY OF CALIFORNIA, SAN DIEGO UCSD

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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

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LA JOLLA, CALIFORNIA 92093
PHONE: (858) 534-2230
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November 22, 2019

Arizona State University
School of Electrical, Computer and Energy Engineering
650 E Tyler Mall, Tempe, AZ 85281

Dear Chair and Members of the Faculty Search Committee,

I am writing to apply for the tenure-track position at the assistant professor level in the School of Electrical, Computer and Energy Engineering at the Arizona State University. I will graduate with a Ph.D. degree in May 2020 from the Department of Computer Science and Engineering at the University of California San Diego.

My research expertise is well aligned with your search interests in the area of circuit for IoT and Edge Computing. Specifically, my research objective is to dramatically increase the learning capability as well as the computing efficiency of today's embedded systems. This includes not only accelerating machine learning algorithms in hardware, but also redesigning the algorithms using strategies that more closely model the ultimate efficient learning machine: "the human brain". My Ph.D. research, with Professor Tajana Rosing (UC San Diego) and Professor Jan Rabaey (UC Berkeley), has been instrumental in developing practical implementations of Hyper-Dimensional (HD) computing - a computational technique modeled after the brain. The Hyper-Dimensional computing system enabled large-scale learning in real-time on embedded devices, including both training and inference. My research showed how HD computing mimics several desirable properties of the human brain, including: robustness to noise and hardware failure, and single-pass learning. These features make HD computing a promising solution for: (i) today's embedded devices with limited storage, battery, and resources, as well as (ii) future computing systems in deep nanoscaled technology, which will have high noise and variability.

My Ph.D. research has been published in over 60 papers in top conferences/journals and opened a new direction for designing intelligent, fast, efficient, and reliable learning systems. My contributions during Ph.D. resulted in over $40M grants funded from multiple governmental agencies and several companies, including IBM, Intel, Micron, Sony, Samsung, Qualcomm, and ARM. I have actively assisted my advisor and contributed to four successful proposal grants funded by the National Science Foundation (NSF) and three grants funded by Semiconductor Research Cooperation (SRC). As a graduate student, I have received the most prestigious awards from both Computer science department and school of engineering at UC San Diego. In 2019, my research has been recognized with the Bernard and Sophia Gordon Engineering Leadership Award, the Outstanding Researcher Award, and the Powell Fellowship by the Jacob School of Engineering (among over 1.4K graduate students). I have also received the Best Doctorate Research in Computer Science at UC San Diego in 2018, the Best Presentation Award in 2019 PhD Forum at Design Automation Conference (DAC), and several Best Paper Nomination Awards at multiple conferences including DAC 2019 and International Symposium on Quality Electronic Design (ISQED 2018).

I have been a teaching assistant (TA) for eight different courses. I also taught three courses as the primary instructor during my Ph.D. study at UC San Diego. I have been strongly recommended by 98.1% of students in the post-class instructor evaluation, which put me among the most popular computer science instructors at UC San Diego. I would like to contribute to your department's mission by (1) covering computer science/engineering courses pertinent to my research areas such as digital systems, embedded system, Internet of Things, computer architecture, machine learning; and (2) developing new graduate-level courses such as machine learning acceleration, brain-inspired computing, and alternative computing paradigm. These courses can provide great ground knowledge

about machine learning by coupling algorithms, computer architecture, and technology.

In addition, during my Ph.D., I was involved in multiple undergraduate and graduate research programs, where I have mentored over 22 undergraduate and 20 graduate students, including 8 Ph.D. students. The mentoring and collaborative experience have not only led to joint research publications but also prepared me for a faculty position. I have also volunteered to be involved in various undergraduate and underrepresented minority (URM) research programs, including ERSP (Early Research Scholarship Program) and ENLACE (Latino Student). The outcome of this mentorship has been published in several papers in top computer engineering journal/conference venues and highlighted by multiple news stations at UC San Diego.

My future research will focus on building efficient and learning-capable IoT devices that can natively support cognitive tasks, beyond the classical machine learning problems, to enable edge intelligence. My research is going to create a new technical foundation that engenders key characteristics of the brain: (1) supports human-level cognition rather than only conventional machine learning tasks, (2) enables efficient and on-the-fly learning on resource-constraint embedded devices, ultimately on processing in-memory architecture. In order to provide a few orders of magnitude efficiency improvements over today's machines, I am planning to design a full-system stack that enables massive concurrency and provides fast computation and data connectivity in a brain-like chip. I also intend to develop a cross-layer processing in-memory architecture that accelerates a wide range of popular learning and data processing procedures. My target applications will be on comprehensive learning with big data, security, and robotics.

In summary, my strong background and experience in both electrical engineering and computer science will make me a valuable addition to your department. Through the demonstrated experiences, I have full confidence to embark on a successful academic career as a faculty member in your department. Enclosed, please find my curriculum vitae (including the list of references), my research, teaching, and diversity statements.

Please do not hesitate to contact me if you need any further information. Thank you for the kind consideration. I am looking forward to hearing from you.

Respectfully yours,

Mohsen Imani

Mohsen Imani
Department of Computer Science and Engineering
University of California San Diego, La Jolla, CA, 92093
Tel: (619)549-9084, Email: moimani@ucsd.edu

Teaching Statement

Mohsen Imani | University of California San Diego

I have been fortunate to experience the joy of learning, innovating, and teaching both as an undergraduate and as a graduate student. During my Ph.D., I was involved in both teaching as a primary instructor and mentoring more than 22 undergraduate and 20 graduate students for various research topics. Now, I would like to continue this joyous adventure as a faculty member. To me, teaching adds to the clarity of thought, which is not only an essential element to one's research endeavor, but also an indispensable element for providing occasions to closely interact with students and engaging them in searching for creative solutions. That being said, I believe that academic teaching is a challenging endeavor, but it is of paramount importance to shape the future of the world. My teaching objective is to help students gain fundamental knowledge, facilitate the acquisition of life-long learning skills, develop analytical reasoning, and prepare them to build successful careers in either industry or academia.

Teaching Philosophy: My philosophy of teaching is to *focus on the students*. I believe successful teaching strategies should centralize around the following goals: (1) teaching in an interactive environment where students can freely involve themselves in the course, (2) encouraging students to ask questions and help them develop skills to find answers and solutions through exploration, and (3) promoting critical thinking skills and retain knowledge that leads to self-actualization. All my teaching and mentoring approaches are aligned with this philosophy and I truly believe in Nico Habermann's philosophy of working with students, "*focus on the students, since graduating great students means you will produce great research, while focusing on the research may or may not produce great students.*" In my experience, the key to achieve the above goals is with ***interactive learning and hands-on projects***, both in class and after class. I always try to first listen to students and realize the basis of their confusion. This allows me to address the real cause of the problem and make my teaching more efficient. I am very hands-on during the beginning of project-based courses; I would explain the base code and walk through simple examples. Once students are on the right path, I asks them to independently explore and solve problems. I believe this strategy can help students to gain confidence and learn how to tackle the projects that seem hard initially.

As a teacher, I strive to engage and inspire growth in my students. I believe every student is capable of benefiting from my passion for theory, research, and practice. I prefer to teach through demonstrations: by conducting real-world examples, analyzing data in the classroom, and participating in an interactive discussion. I teach with the belief that every student possesses unique capabilities that can be shared with others if given the appropriate support. Therefore, I challenge my students to share opinions in groups, so they can learn from each other.

Teaching Experience: I have prepared myself through many teaching experiences during undergraduate and graduate school. I have been a teaching assistant (TA) for eight different courses during the last six years. I also taught three courses as the primary instructor during my graduate study.

Teaching Assistant: Since my undergraduate study, I have had the chance to be heavily involved in teaching courses and mentoring students. In the second year of my undergrad, I started to work as a TA at the University of Tehran for the basic undergraduate course "*Introduction to Electrical Engineering*" with over 100 students. This experience was the starting point in my teaching career. After that, during my third and fourth year of my undergraduate program, I continued to work as a TA in various courses including *Basic Electronic I* and *Basic Electronic II*. During my master program at the University of Tehran, I expanded my teaching experience in different departments including computer science and mechanical engineering for interdisciplinary courses such as *Electronic circuit I* and *II*, graduate courses of *MEMS & NEMS*, *Communication Systems*, and *Linear Control Systems*. As a TA, I was responsible to give lectures in discussion sections, manage the lab sessions, design and grade homework, and hold office hours. All of my assistantships at the University of Tehran were volunteered positions without pay. In 2014, in recognition of all of my hard work as a TA, I was honored to be chosen as the best Teaching Assistant at the University of Tehran, based on the votes of 400 undergraduate students in the Electrical and Computer Engineering department. After joining UC San Diego as a Ph.D. student, I continued teaching by working as a head TA in one of the basic computer science courses: *CSE 140: Digital Design* with more than 300 students from both computer science and electrical engineering departments. In addition to my routine duties as a TA, I was managing a group of 5 TAs and 12 tutors in that course. At the end of the course, I was honored to be strongly recommended by 95% of students as a TA, [1].

Instructor: At UC San Diego, I had a unique opportunity to teach three courses as the primary instructor. In summer 2017, I had been selected to teach two undergraduate courses; *CSE 140: Digital Design* and *CSE 140L: Digital Design Laboratory*. I had over 60 students in each course, and I was managing a group of 8 TAs and Tutors. During these two courses, I always tried to teach through demonstrations: by conducting real-world examples, analyzing data in the classroom, and participating in an interactive discussion. I also challenged my students to share opinions in groups, so they can learn from each other. At the end of quarter, my passion about what I was teaching and how to inspire students resulted in me being strongly recommended by 98.1% of the students (in both courses) for being "well prepared", "very experienced", "with ability of clearly illustrating teaching content", and "good constructive criticism" [2, 3]. This level of satisfaction put me among the most popular instructors who have taught the same courses during the last 20 years at UC San Diego. Last fall, I also had the opportunity to design a new course at UC San Diego, *CSE 291: Alternative Computing Paradigm*, that was offered for graduate students. I was a co-instructor of the course with Professor Tajana Rosing at UC San Diego, where we covered different topics related to emerging computing approaches including

machine learning, quantum computing, DNA computing, and brain-inspired computing.

Mentoring Experience: During my Ph.D., I was involved in multiple undergraduate and graduate research programs in both computer science and electrical engineering departments. I was very lucky to have the chance to ***mentor over 22 undergraduate and 20 graduate students***. This includes directly mentoring 8 Ph.D. students whose projects cover from low-level VLSI design up to architecture and application level. As a mentor, my leading goal was to help students grow as independent researchers and gain important research capabilities and skill sets including: critical thinking, writing, presentation, and collaboration.

Thesis Mentored: Thanks to my Ph.D. advisor, I have had the unique opportunity to mentor three master and two Ph.D. theses at UC San Diego. I have mentored the master thesis of Dr. Daniel Peroni and Max Masich in the Computer Science Department and Saransh Gupta in the Electrical Engineering Department. I also successfully mentored two Ph.D. theses for about four years at UC San Diego; Dr. Daniel Peroni, and Dr. Joonseop Sim. It is very enjoyable to see that both of my mentees are now graduated and joined top industry groups as senior researchers. I would like to repeat this joyful experience with my future students and train highly skilled successful researchers for tomorrow.

Undergraduate Research: I have volunteered to be involved in various undergraduate research programs. In particular, I had interest in ***underrepresented minority (URM) and diversity of academic culture***. I participated in ERSP(Early Research Scholarship Program) and ENLANCE (Latino Student), where I directly mentored over 20 undergraduate and URM students. The mentoring activities included meeting with them periodically, assigning them research projects, designing research experiments, writing co-authored papers, and oral/poster presentations in conferences. The result of this mentorship has been published several papers in top computer engineering journal/conference venues (published with 21 individual undergraduate and 15 URM students [4]). During my mentorship, I was always encouraging my students to continue the higher level education. As a result, eight of my undergraduate students have decided to continue graduate study, and got admitted in top schools including UC San Diego, Carnegie Mellon University, the University of Pennsylvania, and the University of Chicago. In addition, over 14 of my students joined top industry companies including Intel, Amazon, Google, and Apple (List of students are available on my webpage). The outcome of my mentorship has been highlighted by several news outlets at UCSD and the computer science department including UCSD TV [5].

Leadership & Grants: I have actively assisted my advisor and contributed on several grants funded at UC San Diego. Based on the research I have started, our group received four grants from the National Science Foundation–NSF (CSR 1527034, FET 1911095, CHASE-CI 1730158, CC 1826967) and three grants from the Semiconductor Research Cooperation–SRC (JUMP CRISP, Team Project), and SRC/Intel Project), a total of $\$40M$ [6]. For each grant, I led a group of 5-6 Ph.D. students with different research backgrounds in order to write a unified proposal which developed solutions for real-world problems in the computing area. which developed solutions for real-world problems in the computing area. In addition, DARPA recently opened a new program, *"Hyper-Dimensional Data Enabled Neural Networks (HyDDENN)"*, which is entirely based on my Ph.D. thesis [7]. My research has also opened collaboration with seven industrial companies (Intel, IBM, Micron, Qualcomm, SONY, Samsung, and ARM) and several schools including UC Berkeley, UC Irvine, University of Notre Dame, MIT, EPFL, and ETH.

Teaching Interests and Plans: My teaching interests include VLSI systems design, electronic circuit design, logic design, digital systems, computer architecture, embedded systems, and machine learning at all levels. I am qualified and very confident to teach most undergraduate-level courses in electrical/computer engineering and graduate-level courses related to my research interests. In addition, my background in both electrical engineering and computer science makes me well-positioned to design and offer new courses on machine learning for computer architecture and systems, such as machine learning acceleration, alternative computing paradigm, brain-inspired computing, and architecture for big data acceleration in the graduate level. These courses will provide a deeper understanding of learning algorithms with a focus on efficient and robust hardware implementation.

In summary, I strive to be an academic professional who is not only an outstanding researcher but also an excellent developer of minds. I dedicate myself to engineering education to prepare the industry professionals and academic researchers of tomorrow.

References

[1] "Student ASE Evaluation for Mohsen Imani at TA for CSE 140 - Components Design Techniques for Digital Systems. University of California San Diego, Fall 2015." http://moimani.weebly.com/uploads/2/3/8/6/23860882/imani_mohsen_instructor_ia_evaluation_-_cse_140_-_component_desgn_tech_digtl_sysm.pdf and http://moimani.weebly.com/teaching.html.

[2] "Student ASE Evaluation for Mohsen Imani as an **Instructor** for CSE 140 - Design Techniques for Digital Systems. University of California San Diego, Summer 2017." http://moimani.weebly.com/uploads/2/3/8/6/23860882/cse140_evaluation.pdf and http://moimani.weebly.com/teaching.html.

[3] "Student ASE Evaluation for Mohsen Imani as an **Instructor** for CSE 140L - Digital Systems Laboratory. University of California San Diego, Summer 2017." http://moimani.weebly.com/uploads/2/3/8/6/23860882/cse140l_evaluation.pdf and http://moimani.weebly.com/teaching.html.

[4] "List of Student and Publications by Undergraduate and Underrepresented Minority students Mentored by Mohsen Imani, University of California San Diego." http://moimani.weebly.com/diversitylist.html and http://moimani.weebly.com/diversity.html.

[5] "UCSD TV Mirrored Mohsen Imani Mentorship for Latino Student through the ENLANCE Program, University of California San Diego." https://www.youtube.com/watch?v=4CWYIVu3w3w.

[6] "List of Funded Grants Led by Mohsen Imani at University of California San Diego." https://cseweb.ucsd.edu/~moimani.

[7] "DARPA 2019 Call for Proposal: Hyper-Dimensional Data Enabled Neural Networks (HyDDENN)." https://beta.sam.gov/opp/cc3485d29855442f8b406f8dce484670/view.

Research Statement

Mohsen Imani | University of California San Diego

With the emergence of the Internet of Things (IoT), sensory and embedded devices are generating massive data streams. Running big data processing algorithms, e.g., learning, on embedded devices poses substantial technical challenges due to limited device resources. The goal of my research is to dramatically increase the computing efficiency as well as learning capability of the today's computers. My work identifies opportunities for designing ***future learning and computing*** techniques, which are intelligent, fast, efficient, and reliable. I am interested in technology-driven innovations to enable learnability on computing architectures and at the system level.

The traditional von Neumann architecture has a fundamental issue of data movement costs because processing units and memory are separate. My belief is that we will be able to design better computing systems by more closely imitating the ultimate efficient machine, "the human brain", which integrates memory functionalities with computation functionalities. In this sense, my prominent approach is to design brain-inspired algorithms based on the hardware and technology requirements. During my Ph.D. research, I have focused on how to design highly-efficient and reliable learning/computing systems. To make an impact, my research builds practical solutions and applies them to real-world systems. I, therefore, regularly interact with developers from commercial companies while processing their feedback and opinions. As a graduate student, I have received the most prestigious awards from both Computer science department and school of engineering at UC San Diego. In 2019, my research has been recognized with the Bernard and Sophia Gordon Engineering Leadership Award, the Outstanding Researcher Award, and the Powell Fellowship by the Jacob School of Engineering (among over 1.4K graduate students). I have also received the Best Doctorate Research in Computer Science at UC San Diego in 2018, the Best Presentation Award in 2019 PhD Forum at Design Automation Conference (DAC), and several Best Paper Nomination Awards at multiple conferences including DAC 2019.

1. Dissertation Research

1.1. Brain-inspired Hyper-Dimensional Computing: My Ph.D. research, with Professor Tajana Rosing (UC San Diego) and Professor Jan Rabaey (UC Berkeley), has been instrumental in developing practical implementations of Hyper-Dimensional (HD) computing [1, 2] - a computational technique modeled after the brain [3]. The Hyper-Dimensional computing system enabled large-scale learning in real-time, including both training and inference. I have developed such a system by not only accelerating machine learning algorithms in hardware but also redesigning the algorithms themselves using strategies that more closely model the ultimate efficient learning machine: "the human brain". HD computing mimics several desirable properties of the human brain, including: robustness to noise and hardware failure and single-pass learning where training can happen in one-shot without any complex gradient computation. These features make HD computing a promising solution for: (1) today's embedded devices with limited storage, battery, and resources, and (2) future computing systems in deep nanoscaled technology, which will have high noise and variability. I exploited the mathematics and the key principles of brain functionalities to create cognitive platforms. My platform includes: (1) novel ***HD algorithms supporting classification, clustering, regression, and reinforcement learning*** which represent the most popular categories of algorithms used regularly by professional data scientist [4, 5], (2) novel ***HD hardware accelerators*** capable of up to three orders of magnitude improvement in energy efficiency relative to GPU implementations [1, 6, 7], and (3) a ***software infrastructure*** that makes it easy for users to integrate HD computing as a part of any system and enable secure distributed learning on encrypted information [2].

My software contributions are backed by efficient hardware acceleration in GPU, FPGA, and processing in-memory (PIM). I have provided libraries for optimized CPU and GPU implementations of HD applications. I also proposed a fully automatic FPGA-based framework [7, 6] that generates efficient hand-optimized Verilog code, which can be customized for a specific user/device constraints such as quality requirements or power budget. I have also leveraged the memory-centric nature of HD computing to develop an efficient hardware/software infrastructure for a highly-parallel analog acceleration [1]. In particular, I exploited the robustness of HD computing ($\sim$30% robustness to failure in the hardware) to design an analog in-memory associative search [1] which checks the similarity of hypervectors in about tens of nano-seconds, while providing a three orders of magnitude improvement in energy efficiency as compared to today's exact processors [1]. I have also implemented HD computing as a part of two real-world IoT systems: Healthy-Aging project (UCSD-IBM Research) and Smart Home project (UCSD-Samsung). Our implementation indicates that HD computing is well suited to address learning tasks in IoT systems. For example, in a smart home application, our distributed learning based on HD computing with 35 Kintex-7 FPGA devices trains 19x faster and 56x more energy efficient than a neural network, while providing the same learning accuracy [2].

Impact: My research opened a new direction in the brain-inspired learning method that involves many different schools, government agencies, and companies, including IBM, Intel, Samsung, Sony, and Qualcomm. We are collaborating with IBM research to use HD computing for general machine intelligence, where computing systems can have human-like memorization and perform context-aware learning. With Sony and Samsung, we are working on mapping HD computing to practical IoT systems, including a smart agriculture and a smart home project. Our project with multiple groups at Intel is focused on exploiting HD computing for the acceleration of self-learning and bioinformatics applications. Additionally, we are working with Qualcomm and DARPA to develop an analog/digital chips, which can break all the guard-bands that we traditionally need for exact computation. My effort in this project convinced the National Science Foundation (NSF) and the Semiconductor Research Corporation (SRC) to put HyperDimensional computing as one of the key topics in their "2019 call for proposals" [8]. In addition, DARPA recently released a new call for proposal, named "*Hyper-Dimensional Data Enabled Neural Networks (HyDDENN)*", which is entirely based on my Ph.D. research [9]. In our group, my contribution also resulted in receiving multiple grants, including a recently funded grant by NSF (# 1911095) and a grant jointly funded by SRC and Intel.

1.2. Deep Learning and Big Data Acceleration: Running data/memory-intensive workloads on traditional cores results in high energy consumption and slow processing speeds, primarily due to a large amount of data movement between memory and processing units. I have designed an emerging non-von Neumann architecture capable of accelerating fundamental big data applications in real-time with orders of magnitude higher energy efficiency [10, 11]. My design accelerates entire applications directly in or near storage-class memory without using complex processing cores. In the hardware layer, my platform supports essential operations inside memory, including SRAM and DRAM, through the memory hierarchy. In the software layer, I designed an integrated software infrastructure that seamlessly orchestrates the hardware structures. My proposed platform can also accelerate a wide range of big data applications including machine learning [10, 11], query processing, and graph processing. One particularly successful application of my design is FloatPIM [10] and RAPIDNN [11], which significantly accelerate state-of-the-art Convolutional Neural Networks (CNNs). The prominent impact of FloatPIM is that it precisely computes both training and inference phases with *digital* data stored in the storage class memory. FloatPIM achieves up to 5.1% higher classification accuracy as well as 4.3$\times$ speedup and 15.8$\times$ higher energy efficiency, as compared to the state-of-the-art architecture.

Impact: My research in close collaboration with Micron, Intel, and IBM opened a new direction in the area of non-von Neumann architecture. Based on the research that I have started, our group (PI: Tajana Rosing) has received two grants from NSF (#1527034 and #1826967) and

two grants from SRC. In the first SRC project, I actively contributed to the proposal, which has been funded $40M by the Joint University Microelectronics Program (JUMP-CRISP). In the second funded project from SRC, I led writing a proposal that aimed to enhance the software support of my digital-based platform (collaboration with Dr. Samira Khan at the University of Virginia).

2. Future Research Directions

My long-term goal is mainly centered around building a brain-like cognitive machine which tightly couples cognitive functions with the capability of massive data processing. To reach this goal, my plans are (1) revisiting learning algorithms and intelligent use of alternative computing paradigms, and (2) designing a full-system stack which enables massive concurrency and eliminates the data movement. bottleneck of today's von Neumann architecture.

2.1. Brain-like Cognitive Processor: My vision is that the next generation of computers natively supports cognitive tasks, beyond the classical machine learning problems. In my prior work [1], I showed that mimicking brain functionality could improve the energy efficiency and reliability of today's computing systems. My challenge is to create a new technical foundation that engenders three key characteristics of the brain: (1) supports human-level cognition rather than only learning tasks, (2) enables on-the-fly learning on resource-constrained embedded devices and ultimately on memory-centric architectures, and (3) supports self-learning systems which operate without prior knowledge for offline training. I intend to build a cognitive processor that enables brain-inspired computation as a part of the next generation of computing platforms. The processor needs to support cognitive tasks including *memorization, combining, reasoning, association*, as well as *learning*. To enable such general intelligence, I already started working with multiple industry partners and universities to build a system capable of self-learning from an unknown environment. I aim to exploit the advantage of multiple brain-inspired methods, such as neural networks and HD computing models.

In order to address a few orders of magnitude efficiency improvements over today's machines, we require fast computation as well as communication. *Sparse Concurrent Computing:* The existing high-performance processors are designed to compute all parallel components precisely, whereas the brain works in a highly sparse fashion, i.e., meaning that it does not activate all neurons to process tasks. I am planning to enable efficient computing by mimicking this characteristic of the brain. To this end, my next goal is to redefine a brain-like computing paradigm including governing mathematics in a sparse high-dimensional space and a next-generation processor design that efficiently enables the sparse computation. I plan to design a fully analog and highly parallel processor with variable precisions that can potentially work directly on the signal coming from sensors. *Fast On-Chip Communication:* To enable a complex brain-like structure, different computing units of the chip need to communicate together. I intend to look into the emerging technologies and architectures, e.g., 3D IC integration and photonics, to design large-scale, highly connected brain circuits.

2.2. Scalable IoT Edge Intelligence: My goal is to design a hierarchy-aware learning solution which performs the online training and inference in a highly distributed and cost-effective way. At the device level, I am planning to exploit a lightweight learning method that can accurately analysis various data existing in IoT applications, from numerical feature vectors to complex image types. At the system level, I am going to design a novel IoT hierarchy learning technique that enables both training and inference. This includes effective deployment strategies for reliable hierarchy-aware learning, which explicitly considers various network topologies and networking technologies (e.g., WiFi, BLT, and 5G). Additionally, I intend to incorporate active learning in our proposed learning technique to sample the most informative data. My approach is going to: (1) significantly lower data communication between the devices by partially learning on each embedded device, (2) guarantee the scalability and real-time response by avoiding data transfer from embedded devices to the powerful computing environment, and (3) learn adaptively depending on the user's feedback at runtime. I intend to look at the practical implementation of our system in real-world problems, including Healthcare, Wearables, and other cyber-physical systems.

2.3. Efficient Big Data Processing: To provide a real-time response in IoT systems, we need to provide efficient acceleration of popular data processing procedures on embedded devices and servers. This includes acceleration on existing cores (FPGA/GPU/ASIC enhanced with high-bandwidth memory) or emerging architectures. My target applications are in: (1) *Comprehensive Learning with Big Data:* I am interested in accelerating learning algorithms that are beyond existing convolutions neural networks. My focus will be on accelerating unsupervised learning algorithms, reinforcement learning, Bayesian/stochastic learning, and neuromorphic models. That includes accelerating the entire learning method (training and inference) in FPGA/GPU processors and emerging analog/digital architecture depending on the user and application sensitivity to hardware precision. (2) *In-Database Analytic and Graph Processing:* I plan to design an architecture that is going to support highly parallel queries and graph processing where data is stored in storage-class memory. My comprehensive solution requires a co-design of hardware and software and offers high-level easy-to-use user interfaces to define and perform a wide range of analytical data algorithms. (3) *Security Applications:* are the essential workload in today's cloud, emerging mobile, and IoT systems. However, these algorithms take a huge amount of time/energy when running on existing systems. I am planning to provide a highly parallel acceleration of security applications, e.g., encryption and decryption of big data. (4) *Robotics Applications:* are the frontier of artificial intelligence. However, they still lack architectural solutions that enable robotics to self-learn from data available on-the-fly. I am planning to provide a complete stack that maps a specified robotic system to FPGA/ASIC or the cognitive processor that supports brain-like computing.

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