EEE 120 Digital Design Fundamentals (3) [Fall, Spring, Summer Sessions]

Course (Catalog) Description:
Number systems, conversion methods, binary and complement arithmetic, Boolean algebra, circuit minimization, ROMs, PLAs, flipflops, synchronous sequential circuits.
Lecture, lab. Cross-listed as CSE 120. Credit is allowed for only CSE 120 or EEE 120.

Course Type: Required for all electrical engineering majors.
Prerequisite: None
Textbook: *Introduction to Logic Design*, Third Edition, Alan B. Marcovitz, McGraw-Hill, 2010
Supplemental Materials: Laboratory Manual available from course websites (Blackboard LMS) of instructors, Logisim digital circuit simulation software.
Digital Design for the Laboratory: Hardware and Simulation (using LogicWorks™5) Ver. 1, Third Edition, Daniel J. Tylavsky, CenterPoint Publishing, 2003, ISBN 007-295176-1.
LogicWorks 5 by Capilano Computing, Addison Wesley Publishers. (Not required. Available at the Information Techology sites on Campus.)
Coordinator: Dr. Michael Goryll, Professor
Course Objective:

Students will be able to analyze, design, construct, and debug digital combinational logic circuitry and digital finite state machine circuitry.

Course Outcomes:

1. Students will be able to describe the function of electric circuits that perform logic operations using symbols for logic gates or input/output tables (truth tables).
2. Students will be proficient in the use of algebraic equations to describe and analyze Digital Logic circuits and use Boolean Algebra to simplify the circuits.
3. Students will be able to perform algebraic operations in different number systems.
4. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex combinational Digital Logic circuits.
5. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex synchronous machines given a reasonable problem statement.
6. Students will be able to set criteria to determine the "best" design and select the best design.
7. Students will be able to describe the operation of an elementary microprocessor, create an instruction set for an elementary microprocessor, and enter the instruction set into the processor's instruction PROM. Students will also be able to enter a program in the processor's memory and execute the program.

Course Topics:

1. Logic signals and gates (1 week)
2. Number systems, arithmetic and codes (2 weeks)
3. Boolean algebra and combinational logic (1 week)
4. Karnaugh maps (1 week)
5. Combinational Circuit synthesis (1 week)
6. MSI Combinational Logic (adders, subtracters, multiplexers, decoders) (1 week)
7. Output configurations (open collector, 3-state), Programmable Logic Devices (1 week)
8. Sequential logic and flip-flops (2 weeks)
9. Counters, stacks and registers (1 week)
10. Synchronous State Machines (2 weeks)

11. Microprocessors (2 weeks)

Computer Usage:

In a set of five stages, students use digital logic simulation software (LogicWorks or Logisim) to simulate a simple microprocessor. They start with simple boolean gates, build and simulate the MSI parts including an ALU. Memory is then added and in the final stage the students develop machine code instructions for the microprocessor. Reports are due after each stage.

Laboratory Experiments:

Students complete two tutorials, three hardware laboratory experiments, four simulation laboratory experiments, and one capstone design project. Lab TAs are avialable during open lab hours.

Lab H0: Hardware Tutorial: Using a Prototype Board and Voltmeter
Lab H1: Debugging a Half and Full Adder
Lab H2: TTL Characteristics, Three-state Buffers, Open-collector Buffers
Lab H3: Latches, Flip-Flops, Registers and Counters
Lab S0: Simulator Tutorial: Using Logisim
Lab S1: Half Adder, Increment and Two's Complement Circuit
Lab S2: 4-Bit Full Adder, Multiplexer and Decoder
Lab S3: Arithmetic and Logic Unit
Lab S4: The Microprocessor
Capstone Design Project

Course Contribution to Engineering Science and Design:

On tests students will be presented with problems that require them to design digital logic system based on first principles. In addition the Capstone Design Project requires students to design, implement and test a finite state machine solely based on end user requirements. The students should be able to come up with an independent design and come up with solutions to issues arising, e.g. need for synchronization of input or output signals. By applying analytical tools, students are able to verify that their design performs according to the specifications. The students are graded on presenting a circuit that performs the application.

Course Relationship to Program Objectives:

This course, through work required of our students (i.e., homework, exams/quizzes, and laboratory assignments) supports the following objectives of our program (ABET a,b,c,d,g,k): Being the first course in the Digital Design undergraduate curriculum, students will be introduced to the mathematical fundamentals of logic design and logic minimization **(a)** . Students will learn about essential building blocks of modern Digital Logic Systems such as Multiplexers and Decoders and Programmable Logic Devices. They will also be introduced to sequential logic design which is the fundamental concept behind shift regiters and counters. These in turn make up vital parts of modern Digital Systems employing State Machine Design. Students will conduct experiments that will help to reinforce what has been learned through analysis and interpretation of the data observed **(b)**. Equipped with this knowledge, students will design components of larger Digital Systems, such as an Arithmetic Logic Unit as part of a Microprocessor **(c)**. Students will also be involved in a Capstone project which requires each individualstudent to design a Finite State Machine and document the design process. Thus, the course enhances the individual communication skills **(g)** as well as fosters collaborative work on multidiciplinary teams though group excercises and discussions **(d)**. Modern CAD software tools are employed in homework, labs, and the Capstone project to design, analyze, and evaluate designs (**k,c**).

Person preparing this description and date of preparation: Michael Goryll, May. 2015.