

# **SAMPLE SYLLABUS**

This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class. Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.

## ABET Course Syllabus EEE120

1. **Course: EEE 120 Digital Design Fundamentals**
2. **Credits and Contact Hours:** 3 Credit Hours (lecture), Topics: Engineering
3. **Course Coordinator:** Dr. Michael Goryll, Associate Professor
4. **Textbook:** *Introduction to Logic Design*, Third Edition, Alan B. Marcovitz, McGraw-Hill, 2010.

### **Supplemental materials:**

- Laboratory Manual available from course websites (Canvas LMS) of instructors, “Digital” Java-based and iVerilog digital circuit simulation software.

### 5. **Specific course information**

- a. **Catalog description:** Number systems, conversion methods, binary and complement arithmetic, Boolean algebra, circuit minimization, Programmable Logic Devices, flipflops, synchronous sequential circuits. Lecture, lab. Cross-listed as CSE 120. Credit is allowed for only CSE 120 or EEE 120.
- b. **Prerequisites or co-requisites:** None.
- c. **Required/elective/selected elective:** Required

### 6. **Specific goals for the course**

Students will be able to analyze, design, construct, and debug digital combinational logic circuitry and digital finite state machine circuitry.

#### a. **Outcomes of instruction:**

- i. Students will be able to describe the function of electric circuits that perform logic operations using symbols for logic gates or input/output tables (truth tables).
- ii. Students will be proficient in the use of algebraic equations to describe and analyze Digital Logic circuits and use Boolean Algebra to simplify the circuits.
- iii. Students will be able to perform algebraic operations in different number systems.
- iv. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex combinational Digital Logic circuits.
- v. Students will be able to design, build, debug, and demonstrate the operation of arbitrarily complex synchronous machines given a reasonable problem statement.
- vi. Students will be able to set criteria to determine the “best” design and select the best design.
- vii. Students will be able to describe the operation of an elementary microprocessor, create an instruction set for an elementary microprocessor, and enter the instruction set into the processor’s instruction PROM. Students will also be able to enter a program in the processor’s memory and execute the program.

#### b. **Outcomes of Criterion 3 addressed by the course:**

(1) Students will be introduced to the mathematical fundamentals of logic design and logic minimization, making up vital parts of modern Digital Systems employing State Machine Design.

(2) Students will design components of larger Digital Systems, such as an Arithmetic Logic Unit as part of a Microprocessor.

(3, 5) Students will also be involved in a Capstone project which requires each individual student to design a Finite State Machine and document the design process. This enhances the individual communication skills as well as fosters collaborative work on multidisciplinary teams through group exercises and discussions.

(6) Students will conduct experiments that will help to reinforce what has been learned through analysis and interpretation of the data observed.

(1,2,6) Modern CAD software tools are employed in homework, labs, and the Capstone project to design, analyze, and evaluate designs.

7. **Brief list of topics to be covered**

1. Logic signals and gates (1 week)
2. Number systems, arithmetic and codes (2 weeks)
3. Boolean algebra and combinational logic (1 week)
4. Karnaugh maps (1 week)
5. Combinational Circuit synthesis (1 week)
6. MSI Combinational Logic (adders, subtracters, multiplexers, decoders) (1 week)
7. Output configurations (open collector, 3-state), Programmable Logic Devices (1 week)
8. Sequential logic and flip-flops (2 weeks)
9. Counters, stacks and registers (1 week)
10. Synchronous State Machines (2 weeks)
11. Microprocessors (2 weeks)

**Computer Usage:** In a set of five stages, students use digital logic simulation software (Digital and iVerilog) to simulate a simple microprocessor. They start with simple Boolean gates, build and simulate the MSI parts including an ALU. Memory is then added and in the final stage the students develop machine code instructions for the microprocessor. Reports are due after each stage.

**Laboratory Experiments:**

Five laboratory experiments and one Capstone Design Project. Students have the option to implement their Verilog-based designs on Intel FPGA hardware. Lab TAs are available during open lab hours.

Lab 0: Introduction to the CSE120/EEE120 Lab Tools

Lab 1: Half Adder, Full Adder, 4-bit Incrementer and Adder

Lab 2: Multiplexers, Decoders and the Arithmetic Logic Unit

Lab 3: Registers, Counters and the “Brainless CPU”

Lab 4: The Complete Microprocessor

**Course Contribution to Engineering Science and Design:** On tests students will be presented with problems that require them to design digital logic system based on first principles. In addition the Capstone Design Project requires students to design, implement and test a finite state machine solely based on end user requirements. The students should be able to come up with an independent design and come up with solutions to issues arising, e.g. need for synchronization of input or output signals. By applying analytical tools, students are able to verify that their design performs according to the specifications. The students are graded on presenting a circuit that performs the application.

Person preparing this description and date of preparation: Michael Goryll, June. 2021.