

SAMPLE SYLLABUS

This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class. Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.

ABET Course Syllabus EEE333

1. **Course: EEE 333 Hardware Design Languages and Programmable Logic**
2. **Credits and Contact Hours:** 4 Credit Hours (lecture, lab), Topics: Engineering
3. **Course Coordinator:** ECEE Undergraduate Committee
4. **Textbook:** *The Designer's Guide to VHDL*, by Peter J. Ashenden, 3rd Ed, Morgan Kaufmann Publishers, 2008, ISBN: 9780120887859
Supplemental materials: Instructor notes available from course websites (Canvas LMS), Xilinx CPLD and FPGA design notes, Xilinx FPGA design software (Xilinx ISE with Modelsim or iSim), Digilent FPGA boards.
5. **Specific course information**
 - a. **Catalog description:** Develops digital logic with modern practices of hardware description languages. Emphasizes usage, synthesis of digital systems for programmable logic, VLSI.
 - b. **Prerequisites or co-requisites:** CSE 120 or EEE 120, EEE 202.
 - c. **Required/elective/selected elective:** Selected Elective
6. **Specific goals for the course**
 1. Students can design digital circuits using a hardware description language and synthesis.
 2. Students understand modern programmable logic devices and can use them in practical applications.
 3. Students understand timing and effects of hardware mapping and circuit parasitics.
 - a. **Outcomes of instruction:**
 1. Students can apply logic fundamentals using hardware description languages.
 2. Students understand the difference between procedural programming and hardware description languages.
 3. Students can write synthesizable verilog code describing basic logic elements
 - a. Combinatorial logic.
 - b. Sequential logic.
 4. Students can code state machines in a hardware description language.
 5. Students can analyze and develop basic logic pipelined machines.
 6. Students understand basic programmable logic architectures.
 7. Students can synthesize working circuits using programmable logic.
 8. Students understand sequential and combinatorial logic timing.
 9. Students understand the impact of actual routing and circuit parasitics.
 - b. **Outcomes of Criterion 3 addressed by the course:**
 - (1) Comprehensive lectures address the knowledge of a hardware-oriented HDL primer, such as HDL data types, testbenches, Finite State Machines (FSMs), and memory structures. The knowledge gained in this course can be applied to any VLSI design by using a top-down design methodology.
 - (2) Covers CMOS digital logic, VHDL coding and modeling, synthesis and verification, and FPGA design basics.
 - (2,6) The fundamental learning will be reinforced by realistic examples for each topic and by practical lab exercises.
 - (5) Laboratory teams feature various engineering majors.
7. **Brief list of topics to be covered**

1. Review logic fundamentals, gates, latches, flip-flops and state machines (2 weeks).
2. Verilog HDL fundamentals, simulation, and test-bench design (4 weeks).
3. Synthesizable code and hardware/HDL mapping (3 weeks).
 - a. Basic logic.
 - b. Sequential circuits.
 - c. Arithmetic circuits.
4. CPLD architecture and synthesis (3 weeks).
5. FPGA architecture and synthesis (4 weeks).

Computer Usage: Modelsim or iSim and FPGA synthesis tools.

Laboratory Experiments: Students meet weekly for a three-hour laboratory under the guidance of a TA.

Course Contribution to Engineering Science and Design: EEE 333 contributes to engineering science through logic design, problem solving, and computer solutions.

Person preparing this description and date of preparation: K. Tsakalis, M. Goryll, June, 2021.