

# **SAMPLE SYLLABUS**

This syllabus is to be used as a guideline only. The information provided is a summary of topics to be covered in the class. Information contained in this document such as assignments, grading scales, due dates, office hours, required books and materials may be from a previous semester and are subject to change. Please refer to your instructor for the most recent version of the syllabus.

## ABET Course Syllabus EEE425

1. **Course: EEE 425 Digital Systems and Circuits**
2. **Credits and Contact Hours:** 4 Credit Hours (lecture, lab), Topics: Engineering
3. **Course Coordinator:** Dr. Sule Ozev, Professor
4. **Textbook:** Rabaey, *Digital Integrated Circuits: A Design Perspective*, 2<sup>nd</sup> Prentice Hall, 2002 ISBN: 978-0130909961.  
**Supplemental materials:** Weste and Harris, *CMOS VLSI Design*, Addison Wesley.
5. **Specific course information**
  - a. **Catalog description:** Digital logic gate analysis and design. Propagation delay, fan out, power dissipation, noise margins. Design of CMOS logic families, including static, dynamic and pass-gate logic. Inverter, combinational and sequential logic circuit design, CMOS memories, VLSI circuits. Computer simulations using Cadence.
  - b. **Prerequisites or co-requisites:** EEE335.
  - c. **Required/elective/selected elective:** Elective
6. **Specific goals for the course**

Students will be able to analyze and design digital integrated circuits.

  - a. **Outcomes of instruction:**
    1. Understanding the basic principles of digital circuit design
    2. Being able to analyze digital gates in terms of noise margin, voltage transfer curve, propagation delay, power consumption
    3. Being able to optimize a logic path comprised of logic gates in terms of its delay
    4. Understanding design principles for sequential circuits
    5. Being able to design more complex digital blocks, including registers, adders, multipliers.
    6. Understanding how basic memory cells work and being able to design SRAM and DRAM cells.
  - b. **Outcomes of Criterion 3 addressed by the course:**
    - (1) Students are required to apply mathematics, electrical science, and engineering to successfully complete the class. Models are used for standard processes, so students are exposed to model parameters. They are also proficient in the judicious use of approximations in models for different applications.  
Students are taught problem solving through circuit design, circuit analysis, layout of circuits, extraction of layout parameters, and design analysis. Both homework and laboratory assignments require design and analysis.
    - (2) Students have extensive exposure to modern circuit simulation tools, such as, Cadence tools and PSPICE, used for layout, simulation, and extraction as well as contemporary methods in electronic circuit analysis.
    - (6) Laboratory experiments require data interpretation. Contemporary issues are inherent in the lectures.
7. **Brief list of topics to be covered**
  - CMOS Technology, MOS Transistors
  - Circuit Layout and Design Rules, Transistor Capacitances
  - CMOS Inverter
  - Combinational Logic: Delay Minimization, Logical Effort
  - Pass Gate Logic and Dynamic Logic

- Sequential Circuits
- Clocking and Synchronous Design
- Timing and pipelining
- Adders
- Multipliers, Shifters, and Memory
- Low power design and interconnect issues

**Computer Usage:**

Labs for Cadence simulation of digital circuits, layout of integrated circuits.

**Laboratory Experiments:**

Students meet weekly for a three-hour laboratory under the guidance of a TA.

1. Static CMOS Inverter Characteristics
2. Characteristics of CMOS Inverter
3. Characterization of CMOS NAND and NOR Gates
4. Characterization of CMOS Half-Adder
5. Design of a Half-Adder and a Clocked SR Latch
6. Layout of an NMOS and PMOS Cell
7. Layout and Verification of a CMOS Inverter
8. Layout of a Half-Adder

**Course Contribution to Engineering and Design:**

EEE425 contributes to engineering science through circuit analysis, problem solving, computer simulations, and applications of mathematics, physics, and electronics. Design occurs through homework assignments (6) throughout the semester and in Lab experiment 3.

Person preparing this description and date of preparation: S. Ozev, K. Tsakalis, June, 2021.